

# AM62L EVM (TMDS62LEVM)

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BOARD REVISION	E1-1A
SCHEMATIC VERSION	2.1

### D-Note :-

EVM is processor evaluation board or platform. The EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM while designing their custom board. The information found in the datasheet should always take precedence over the EVM implementation.

### R-Note :-

- \* Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of board design before board assembly
- \* A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor
- \* Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build.(Refer FAQs listed for additional details)

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# REVISION HISTORY

	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	0.01	8 JAN 2024	Initial Draft derived from AM62P SK - PROC164E1-1 schematics	Mistral Design Team	Nishant	Ajit MB
	0.02	11 JAN 2024	Replaced parts : LPDDR4 (2 GB), Updated FT4232 UART section	Mistral Design Team	Nishant	Ajit MB
	0.03	12 JAN 2024	Updated power section & PMIC part as per PDN	Mistral Design Team	Nishant	Ajit MB
	0.04	16 JAN 2024	Added ADC header, MCAN headers & updated respective net connections	Mistral Design Team	Nishant	Ajit MB
	0.05	18 JAN 2024	Updated SoC RTC and SoC Reset section	Mistral Design Team	Nishant	Ajit MB
	0.06	19 JAN 2024	- Updated PMIC 1 and PMIC 2 connections - Updated PMIC local caps, GPIO connections & assembly variants	Mistral Design Team	Nishant	Ajit MB
	0.07	22 JAN 2024	Implemented Internal review comments and shared to TI for Review	Mistral Design Team	Nishant	Ajit MB
	0.08	23 FEB 2024	Implemented Modular approach and shared to TI for the review	Mistral Design Team	Pandiya rajan	Ajit MB
	0.09	15 MAR 2024	Updated Block diagrams and ADC header	Mistral Design Team	Pandiya rajan	Ajit MB
	0.10	19 MAR 2024	Replaced QSPI NAND flash with new part	Mistral Design Team	Pandiya rajan	Ajit MB
	0.11	20 MAY 2024	- Added 0 ohm series resistor to QSPI data lines - Added 2 push buttons for PMIC nWAKEUP logic - Added current monitor for VDDACORE power supply	Mistral Design Team	Pandiya rajan	Ajit MB
	0.12	22 MAY 2024	- Added RC circuit for I2C2_SCL and I2C2_SDA - R169, R210, R217 has been DNI'd - Changed Assembly instruction for R215 and R209 to Mount	Mistral Design Team	Pandiya rajan	Ajit MB
	0.13	11 JUNE 2024	- Added new connections for No RTC mode in J35 - 5x3 Header - Added GPIO expansion connector - Change PMIC input from VCC_5V0 to VCC_3V3_MAIN	Mistral Design Team	Pandiya rajan	Ajit MB
	0.14	02 JULY 2024	Updated decaps of PMIC 1 and PMIC 2	Mistral Design Team	Pandiya rajan	Ajit MB
	0.15	05 JULY 2024	- Added U81 Buck regulator for 2V5 supply - Removed load switch and added AND gate for the enable logic 3V3 and 5V0 Pre-regulators	Mistral Design Team	Pandiya rajan	Ajit MB
	0.16	11 JULY 2024	- Input power supply of VDD_RTC and VDD_RTC_1V8 LDO's has been changed to VCC_3V3_MAIN - RTC mode selection header connections has been updated	Mistral Design Team	Pandiya rajan	Ajit MB
	0.17	22 JULY 2024	- PORz (Power ON reset) logic has been changed - Values of Current sense resistors have been changed	Mistral Design Team	Pandiya rajan	Ajit MB
	0.18	25 JULY 2024	Implemented the TI review comments.	Mistral Design Team	Pandiya rajan	Ajit MB
	0.19	29 JULY 2024	- Shunt resistor R3969, R3968 have been placed between J35 and SOC pin - Shunt resistor R3939 has been removed	Mistral Design Team	Pandiya rajan	Ajit MB
	0.20	05 AUG 2024	- Changed the value of shunt resistor R426 to 0.02E - Changed the values of shunt resistors R164, R4034 to 0.04E	Mistral Design Team	Pandiya rajan	Ajit MB
	0.21	07 AUG 2024	- 1x3 headers (J16, J6, J18) of MCAN have been replaced with 1x4 headers - Changed the package of U47 from 4-Pin X2SON to 5-Pin SOT-23	Mistral Design Team	Pandiya rajan	Ajit MB
	0.22	08 AUG 2024	The schematics has been Back annotated	Mistral Design Team	Pandiya rajan	Ajit MB
	0.23	20 AUG 2024	- All the D-Notes and CAD Notes have been updated - Block diagrams have been updated	Mistral Design Team	Pandiya rajan	Ajit MB
E1-1	1.1	18 NOV 2024	- Changed Assembly instruction for R124, C487 & C489 to Mount - C481 value has been changed from 0.1uF to 1uF - R588 & R594 value has been changed from 10K to 1K	Mistral Design Team	Pandiya rajan	Ajit MB
	1.2	20 NOV 2024	- The enable logic of Bootmode buffers U111, U114 & U110 have been changed by connecting one of the output of IO Expander to U23 AND gate. - PMIC-2 (U50) and its corresponding inductors and capacitors were mounted as TPS65214x PMIC will be using as primary PMIC for the production build. - PMIC-1 (U48) and its corresponding inductors and capacitors were made as NM	Mistral Design Team	Pandiya rajan	Ajit MB
	1.3	21 NOV 2024	J25 and J26 1x2 headers have been added to EXP_PS_3V3_EN and EXP_PS_5V0_EN signals respectively to provide option to select default state of U2 and U4 load switch enable	Mistral Design Team	Pandiya rajan	Ajit MB
	1.4	16 DEC 2024	- J27 & J28 1x2 headers have been added to have the option to short the shunt resistor on VDD_RTC (R505) and VDD_RTC (R516). These two jumpers are DNI'd - SMD TP's are added across the shunt resistor on VDD_RTC (R505) and VDD_RTC (R516) - For the INA devices, supply has been replaced with VCC_3V3_MAIN instead of VCC_3V3_SYS. - Added level shifter U134 for SoC_I2C1_SDA/SCL between SoC & INA devices for shifting IO level between VCC_3V3_SYS and VCC_3V3_MAIN - J29 (1x2 header) has been added to FET_SEL0 signal	Mistral Design Team	Pandiya rajan	Ajit MB
	1.5	17 DEC 2024	Updated R497 to be mounted with a 0ohm resistor and R154 to be DNI.	Mistral Design Team	Pandiya rajan	Ajit MB
	1.6	02 JAN 2025	All the D-Notes, CAD Notes and Block diagrams have been updated	Mistral Design Team	Pandiya rajan	Ajit MB
	1.7	12 MAR 2025	The D-Notes and CAD Notes have been updated	Mistral Design Team	Pandiya rajan	Ajit MB
	1.8	14 MAR 2025	All the D-Notes, CAD Notes and Block diagrams have been updated	Mistral Design Team	Pandiya rajan	Ajit MB
	1.9	21 MAR 2025	The D-Notes, CAD Notes, R-Notes and Block diagrams have been updated	Mistral Design Team	Pandiya rajan	Ajit MB
	1.10	26 MAR 2025	Changed part number of AM62L SoC to XAM62L32AOGHAANB	Mistral Design Team	Pandiya rajan	Ajit MB
	1.11	01 APR 2025	D-Notes and Links to key FAQs have been updated	Mistral Design Team	Pandiya rajan	Ajit MB
	1.12	08 JULY 2025	- D-Notes and CAD Notes have been updated - Added Power Sequence at RTC Only mode	Mistral Design Team	Pandiya rajan	Ajit MB
E1-1A	2.1	06 OCT 2025	Part number of AM62L SOC (U28) has been changed from XAM62L32AOGHAANB to AM62L32BOGHAANB	Mistral Design Team	Pandiya rajan	Ajit MB

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## KEY LINKS TO COLLATERALS

<b>AM62L EVM (TMD62LEVM) :</b> <a href="https://www.ti.com/product/AM62L">https://www.ti.com/product/AM62L</a>
<b>AM62Lx Sitara™ Processors datasheet :</b> <a href="https://www.ti.com/lit/pdf/SPRSPA1">https://www.ti.com/lit/pdf/SPRSPA1</a>
<b>Hardware Design Considerations :</b> <a href="https://www.ti.com/lit/pdf/SPRUJC9">https://www.ti.com/lit/pdf/SPRUJC9</a>
<b>DDR Board Design and Layout Guidelines :</b> <a href="https://www.ti.com/lit/pdf/sprad06">https://www.ti.com/lit/pdf/sprad06</a>
<b>Schematic Design and Review Checklist for AM62Lx processor family :</b> <a href="https://www.ti.com/lit/pdf/SPRAD08">https://www.ti.com/lit/pdf/SPRAD08</a>
<b>SKs (Starter Kits) for reference :</b> SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, TMD62LEVM, SK-AM62A-LP, SK-AM62P-LP

## LINKS TO KEY FAQs

<a href="https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478018/faq-am62l-custom-board-hardware-design-collaterals-to-get-started">https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478018/faq-am62l-custom-board-hardware-design-collaterals-to-get-started</a>
<a href="https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am243x-am62x-am62ax-am62px-am62d-q1-am62l-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review">https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am243x-am62x-am62ax-am62px-am62d-q1-am62l-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review</a>
<a href="https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478030/faq-am62l-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-evm">https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478030/faq-am62l-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-evm</a>
<a href="https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478025/faq-am62l-custom-board-hardware-design---reusing-ti-evm-design-files">https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478025/faq-am62l-custom-board-hardware-design---reusing-ti-evm-design-files</a>
<a href="https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1318441/faq-am625-am623-am62a-design-recommendations-commonly-observed-errors-during-custom-board-hardware-design-sk-schematics-updates-for-design-update-note">https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1318441/faq-am625-am623-am62a-design-recommendations-commonly-observed-errors-during-custom-board-hardware-design-sk-schematics-updates-for-design-update-note</a>
<a href="https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478027/faq-am62l-design-recommendations-custom-board-hardware-design--custom-board-schematics-self-review">https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478027/faq-am62l-design-recommendations-custom-board-hardware-design--custom-board-schematics-self-review</a>
<a href="https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1522815/faq-am62l-am62132-am62131-custom-board-hardware-design--available-design-files-and-supported-cad-tools-format-that-can-be-used-during-custom-board-schematic-and-pcb-design">https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1522815/faq-am62l-am62132-am62131-custom-board-hardware-design--available-design-files-and-supported-cad-tools-format-that-can-be-used-during-custom-board-schematic-and-pcb-design</a>

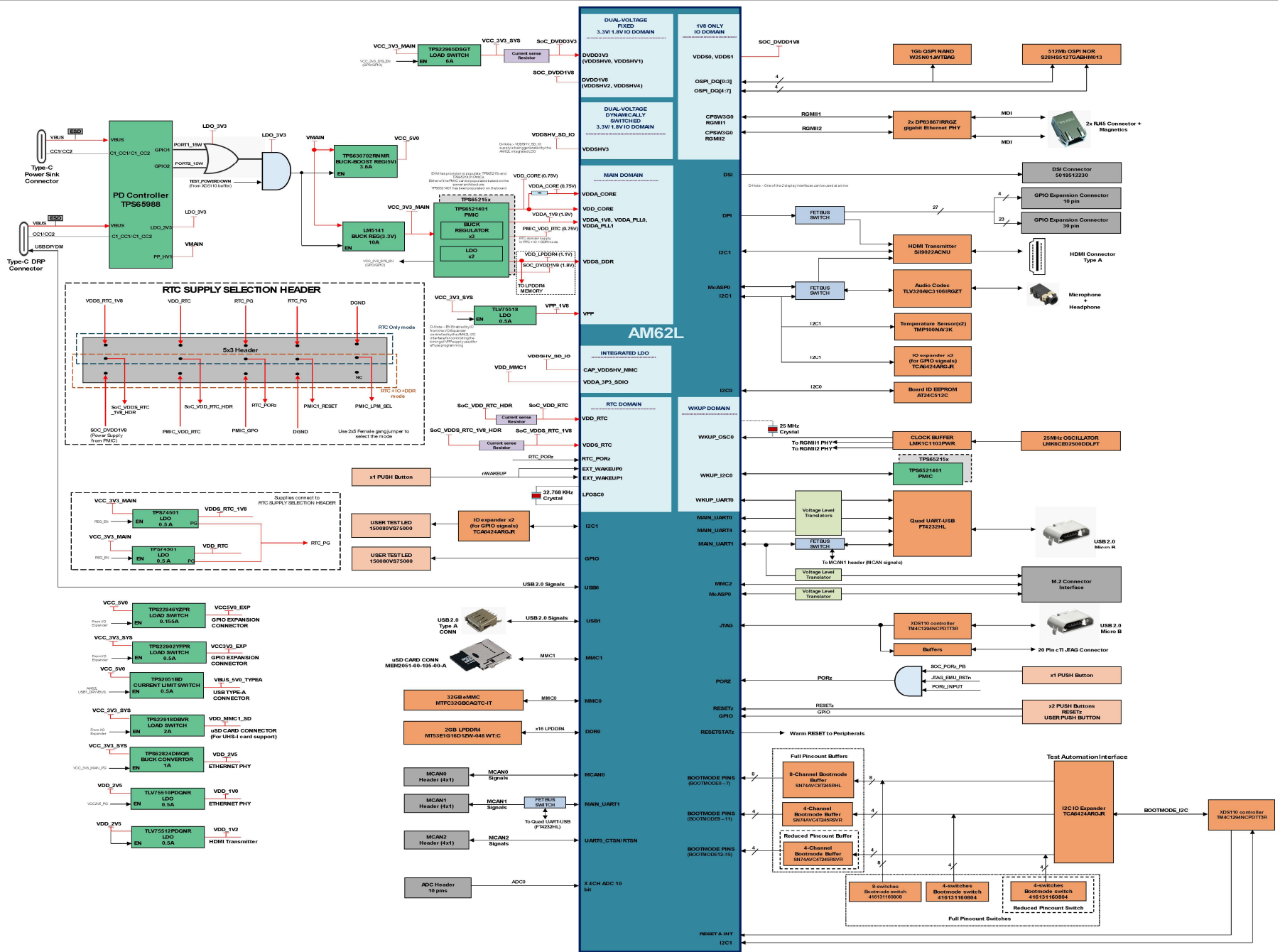
## COMMON SOC LVCMOS IO INTERFACE GUIDELINES

1.	Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.
2.	SOC LVCMOS IOs have slew rate requirements specified, applying a slow ramp input or connecting a cap at the input is not recommended.
3.	Connecting a cap load 50 pF or more at the output is not recommended. DNI cap or perform simulations based on the use case.
4.	SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IO that could float.
5.	Any SOC IO that has a trace connected needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals.
6.	Connecting SOC IOs that have alternate function that can be configured directly to supply or ground is not allowed or recommended (including bootmode inputs). (Customer could have bug with their firmware and mis-configure these LVCMOS GPIOs that were intended to be inputs, to be outputs driven logic high instead).
7.	Verify cap loading of the SOC output (when any cap value > 22 pF (use case dependent, max value) is connected, customer needs to simulate), slew rate of the input signal (LVCMOS input slew should be 1000 ns or less), IO compatibility and fail-safe operation between the SOC IOs and attached devices.

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## BLOCK DIAGRAM - AM62L EVM



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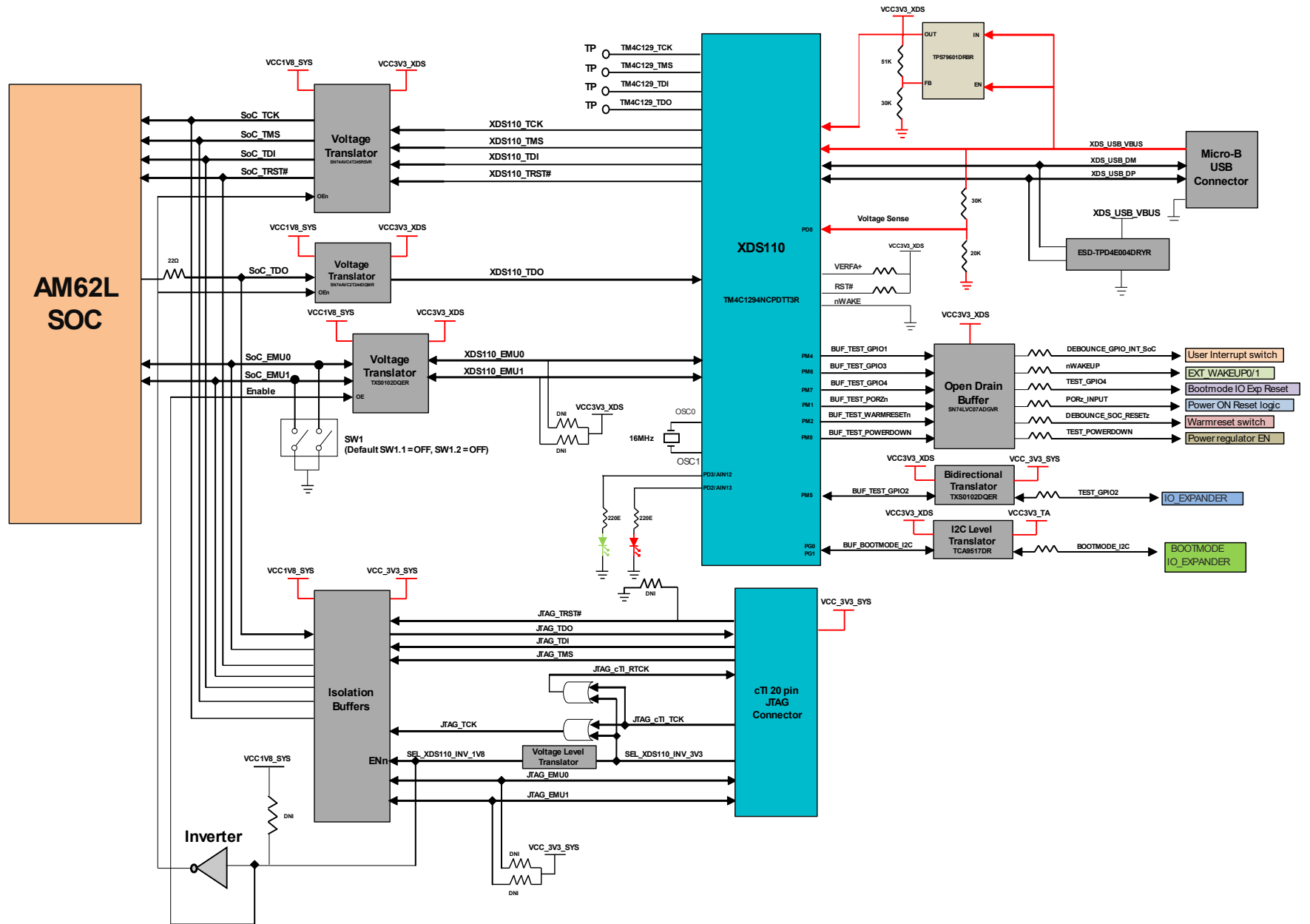
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# BLOCK DIAGRAM - XDS110 DEBUGGER



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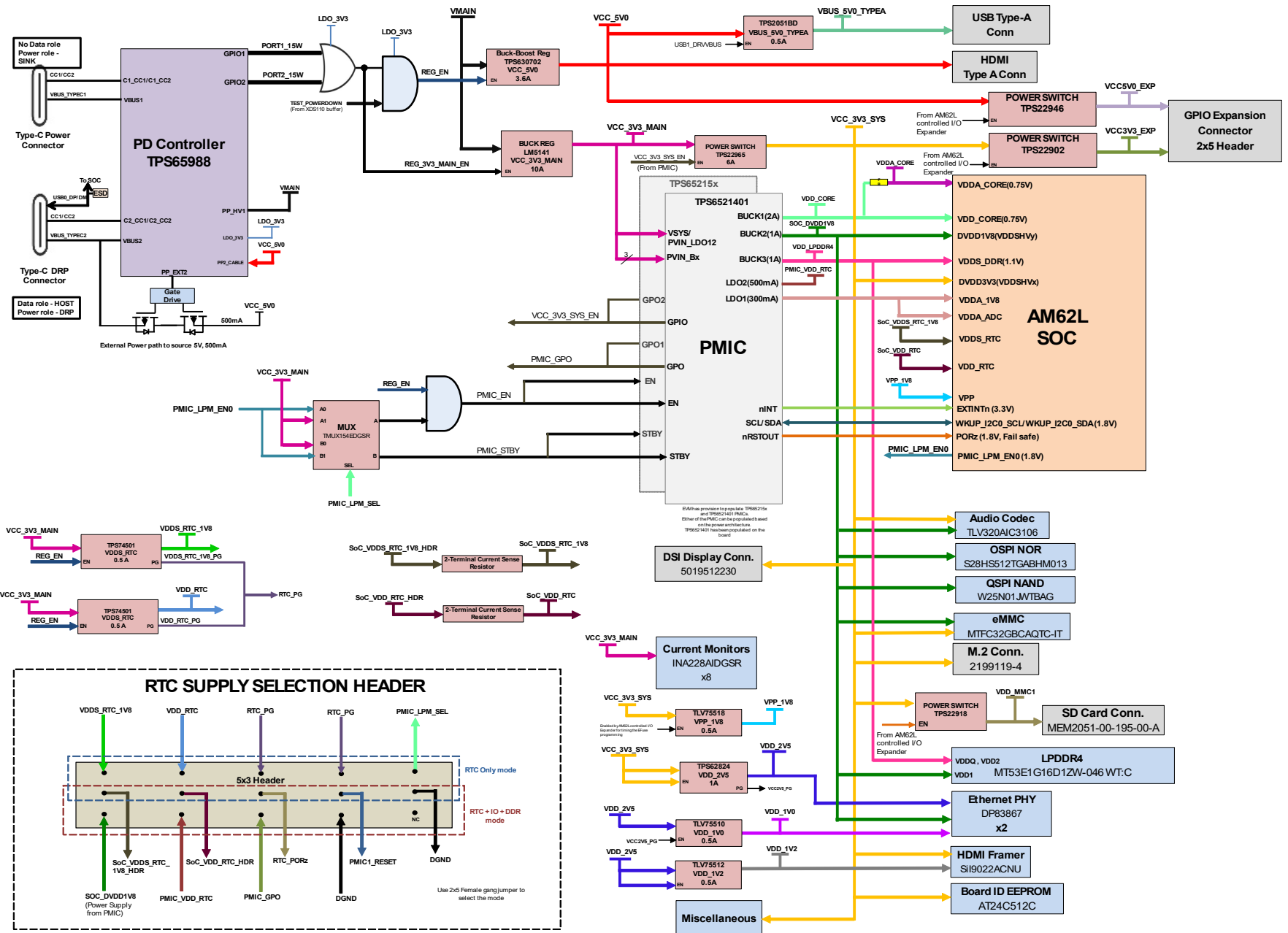
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## POWER ARCHITECTURE BLOCK DIAGRAM



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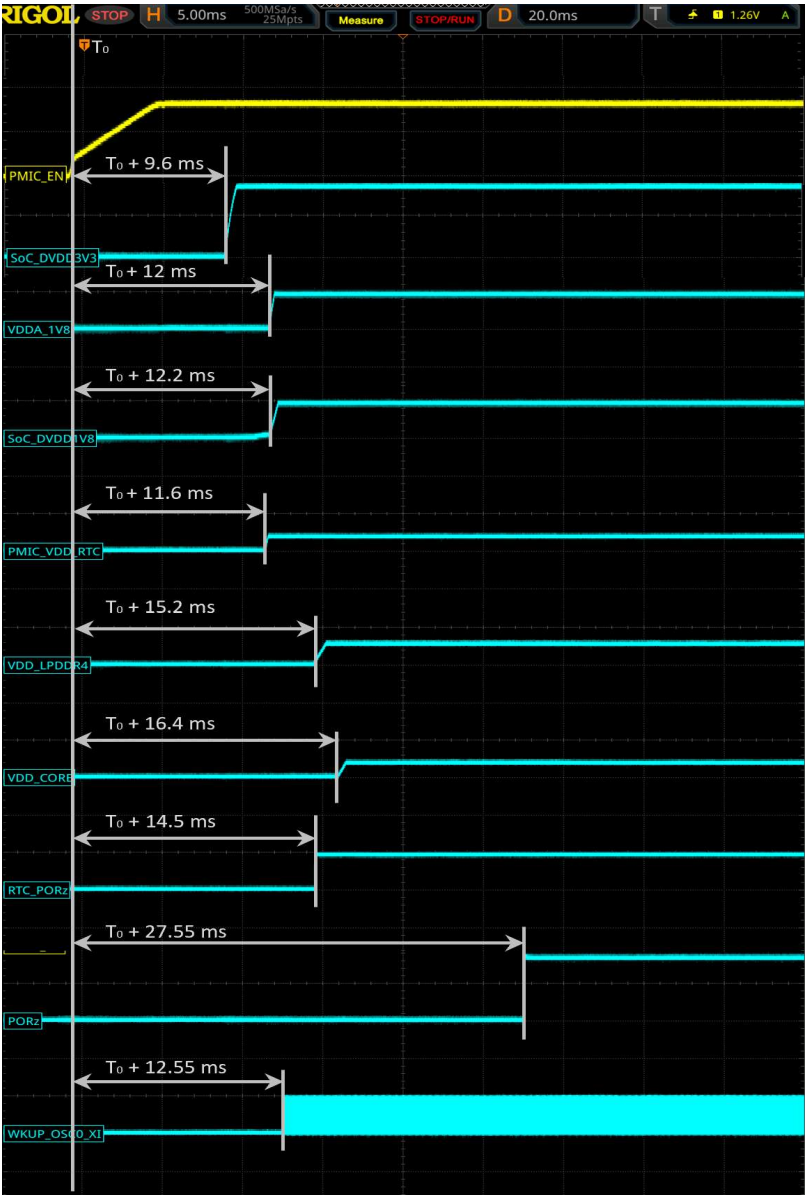
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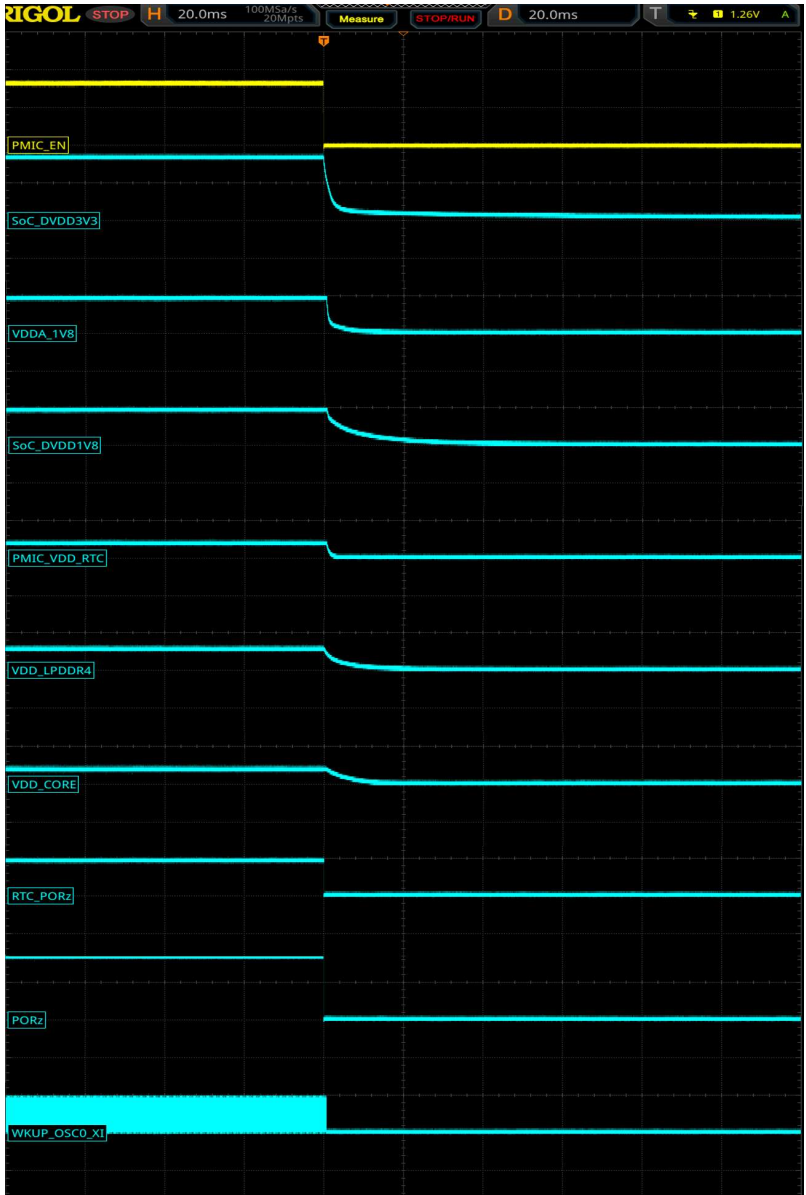
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POWER SEQUENCE - RTC + IO + DDR MODE

POWER-UP SEQUENCE



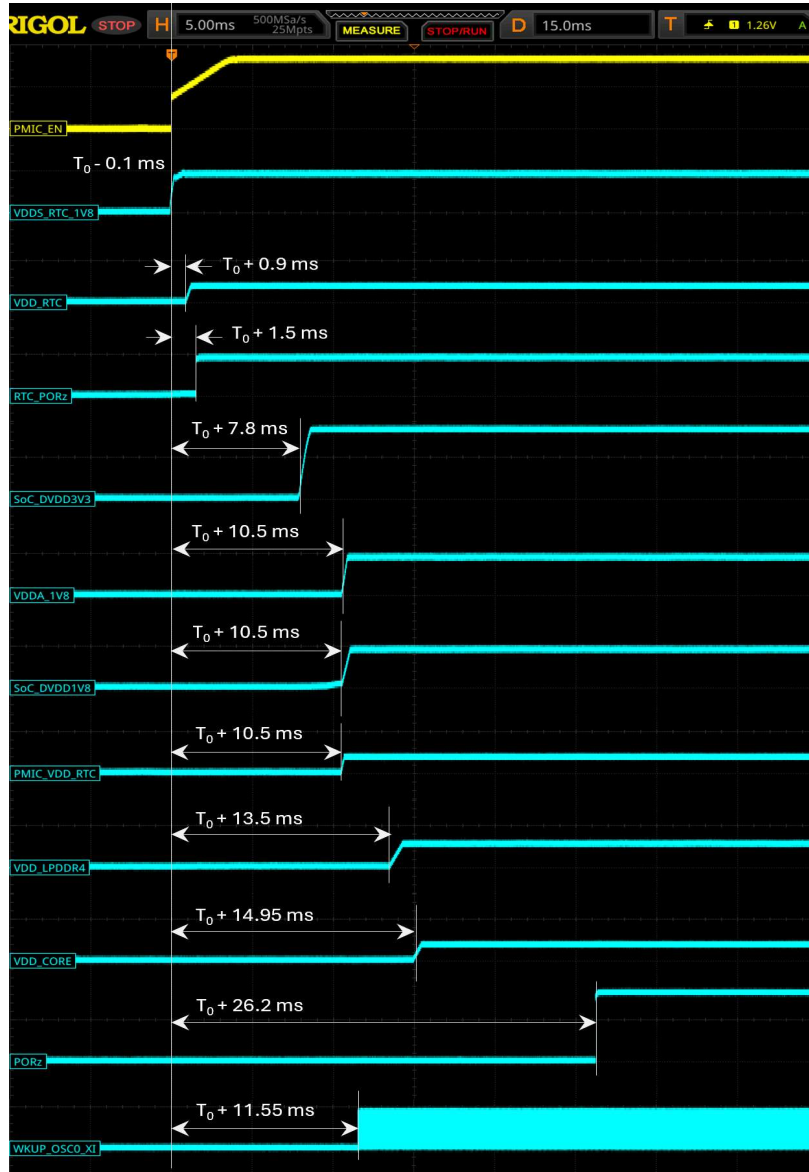
POWER-DOWN SEQUENCE



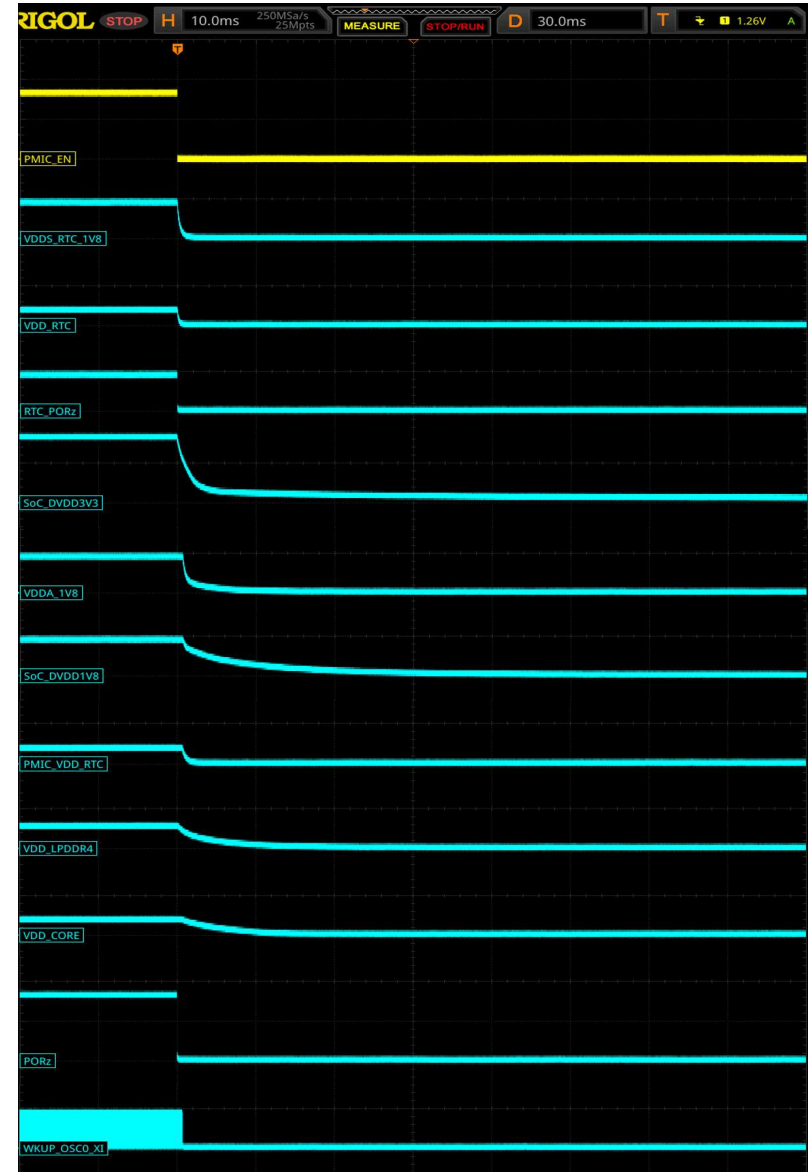


# POWER SEQUENCE - RTC ONLY MODE

## POWER-UP SEQUENCE



## POWER-DOWN SEQUENCE



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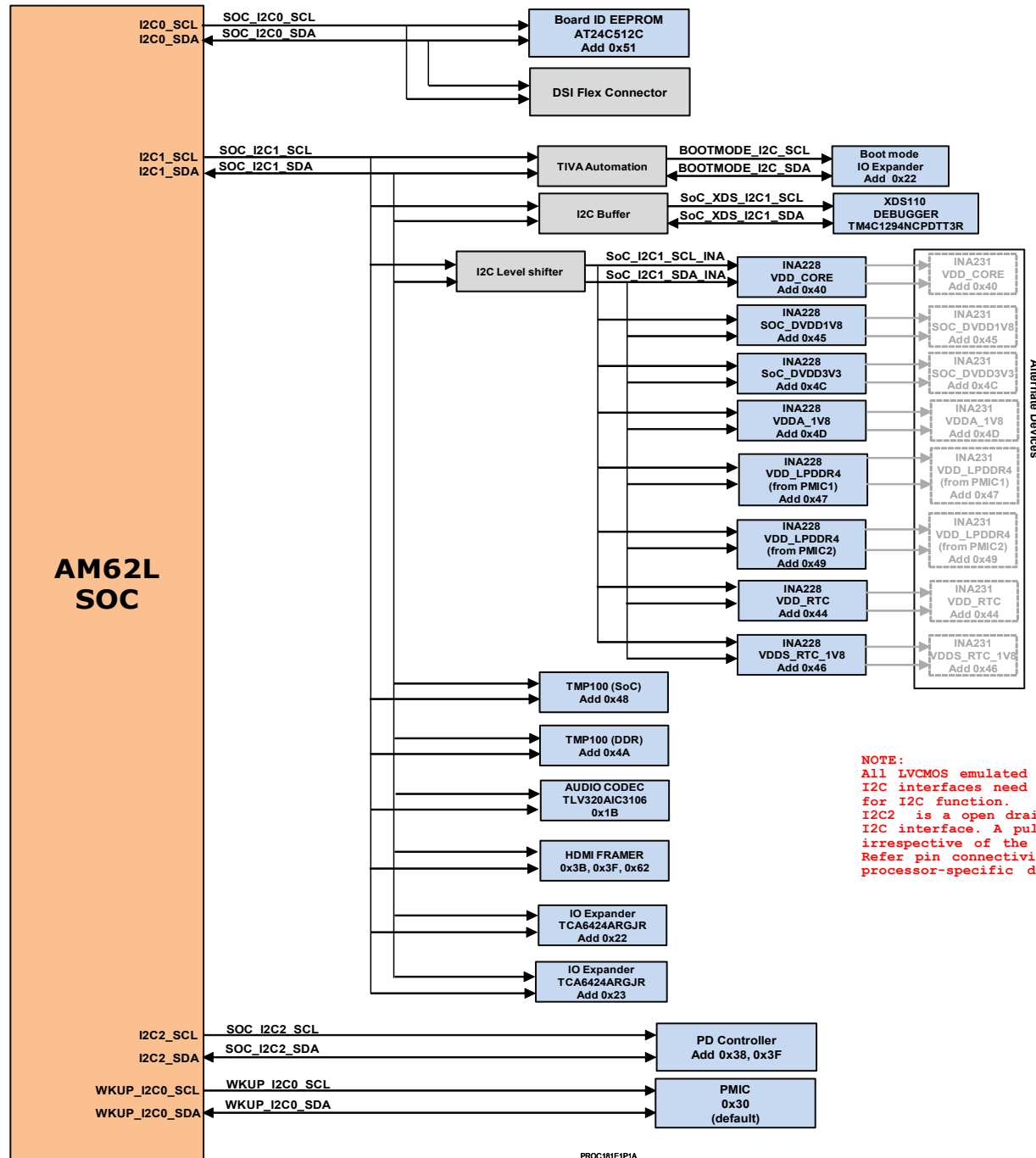
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# I2C TREE



**NOTE:**  
 All LVCMOS emulated open drain output type I2C interfaces need a pullup when configured for I2C function.  
 I2C2 is a open drain output type IO buffer irrespective of the IO configuration, when used. Refer pin connectivity requirements of the processor-specific data sheet.

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# GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NET NAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON EVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_51	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV4	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_52	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV4	SoC_DVDD1V8
3	OSPI NOR Reset Control GPIO	GPIO_OSPI_NOR_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSD1	SoC_DVDD1V8
4	OSPI NOR Interrupt	OSPI_NOR_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSD1	SoC_DVDD1V8
5	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO0_105	EXTINTn	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD3V3
6	IO Expander Interrupt	GPIO0_91_INTn	INTERRUPT	GPIO0_91	SPI0_D1	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD3V3
7	User test LED control signal	SOC_GPIO0_123	ENABLE	GPIO0_123	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV1	SoC_DVDD3V3
8	User Interrupt	GPIO0_90_INTn	INTERRUPT	GPIO0_90	SPI0_D0	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD3V3
9	PMIC Interrupt	PMIC_nINT	INTERRUPT	GPIO0_105	EXTINTn	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD3V3
10	VOUT0 FET switch selection	SoC_VOUT0_FET_SEL1	SELECTION	GPIO0_87	SPI0_CS0	OUTPUT	HIGH	NA	VDDSHV1	SoC_DVDD3V3
11	VOUT0 FET switch selection	SoC_VOUT0_FET_SEL0	SELECTION	GPIO0_89	SPI0_CLK	OUTPUT	HIGH	NA	VDDSHV1	SoC_DVDD3V3
IO EXPANDER – 01										
1	UART1 FET selection control	UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P02		OUTPUT	HIGH	NA		VCC_3V3_SYS
2	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
3	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER-P04		OUTPUT	LOW	HIGH		VCC_3V3_SYS
4	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
5	SOC UART1 Mux Enable	UART1_FET_BUF_EN	ENABLE	IO EXPANDER-P06		OUTPUT	HIGH	LOW		VCC_3V3_SYS
6	DSI Display GPIO0	DSI_GPIO0	GPIO	IO EXPANDER-P10		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
7	DSI Display GPIO1	DSI_GPIO1	GPIO	IO EXPANDER-P11		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
8	BT UART WKUP Signal	BT_UART_WAKE_SOC_3V3	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
9	USB Type A overcurrent indicator	USB_TYPEA_OC_INDICATION	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS
10	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
11	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
12	TEST GPIO2	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
13	MCASP0 Enable and Direction Control	MCASP0_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
14		MCASP0_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
15		MCASP0_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	NA		VCC_3V3_SYS
16	DSI to HDMI Card Device ID interrupt	DSI_EDID	INTERRUPT	IO EXPANDER-P25		INPUT	HIGH	LOW		VCC_3V3_SYS
17	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
18	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER – 02										
1	M.2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
2	VOUT0 FET switch selection	VOUT0_FET_SEL0	SELECTION	IO EXPANDER-P01		OUTPUT	LOW	NA		VCC_3V3_SYS
3	M.2 Interface Level Translator Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P11		OUTPUT	LOW	HIGH		VCC_3V3_SYS
5	QSPI NAND Reset Control GPIO	GPIO_QSPI_NAND_RSTn	RESET	IO EXPANDER-P20		OUTPUT	HIGH	LOW		VCC_3V3_SYS
6	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P21		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P23		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Bootmode Buffer Enable	GPIO_BOOTMODE_BUF_ENz	ENABLE	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC_3V3_SYS
12	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS

PROC181E1P1A

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Title GPIO MAPPING TABLE

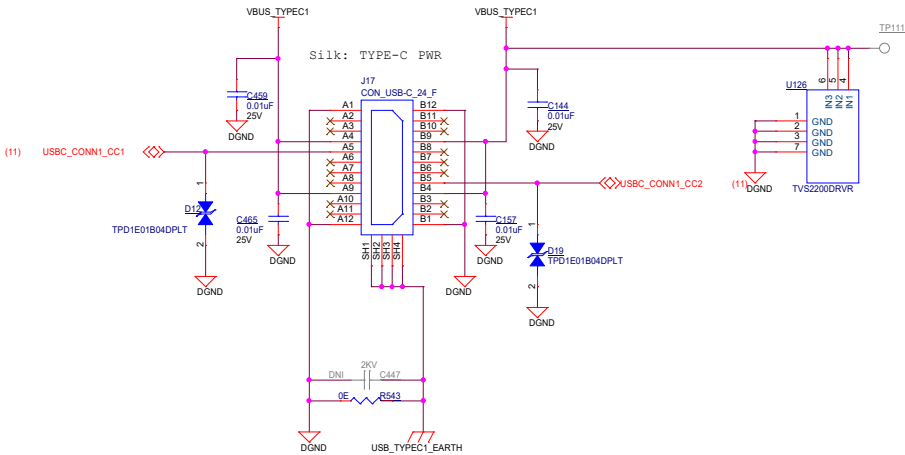
Size	PROC181E1-1A	Rev	E1-1A
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## TYPE-C DUAL PD CONTROLLER

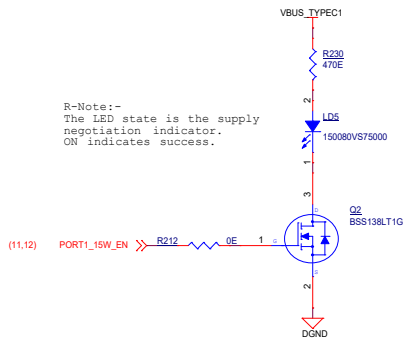


<b>Title</b> USB TYPE-C POWER			
<b>Size</b>	PROC181E1-1A		<b>Rev</b>
C			E1-1A
<b>Date:</b>	Monday, October 06, 2025	<b>Sheet</b>	11 of 56

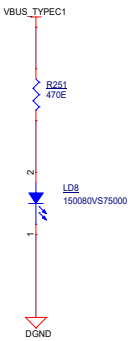
USB TYPE-C POWER CONNECTOR



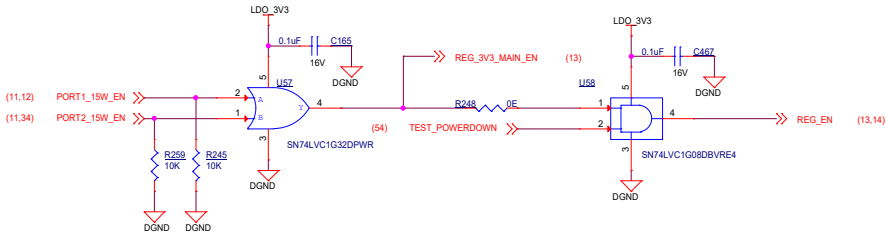
PORT1\_15W\_EN STATUS INDICATION LED



POWER INDICATION LED: VBUS\_TYPEC1



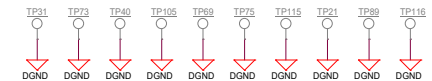
PRE REGULATOR POWER SUPPLY ENABLE LOGIC



D-Note:-  
REG\_3V3\_MAIN\_EN is enabled only when a 15W or above PD negotiation succeeds.  
On custom board designs, ORING logic can be removed when USB PD controller is not used.

D-Note:-  
The TEST\_POWERDOWN is by default HIGH and is used to turn-OFF the PMIC, U63, U107, U113 through on-board XDS110. For custom designs, the ANDING logic can be removed when on-board XDS110 is not used.

```
VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A
```



### 3.3V, 10.0 AMPS SUPPLY

inMin = 4.5V  
inMax = 15V  
out = 3.3V @ 10A

VMAIN

D-Note:-  
VCC\_3V3 MAIN  
Add provision for Jumper or 0R for isolation or  
load current measurement for preproduction boards

CAD Note:  
Follow Kelvin current sense routing

TP102

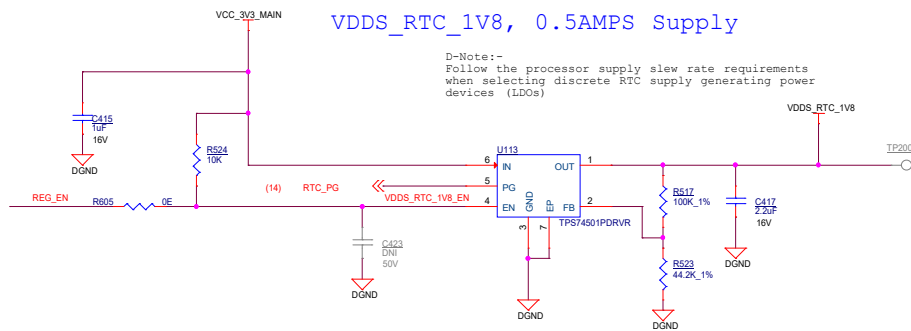
VCC\_3V3\_MAIN

PCB Note:  
Short LM5141\_AGND and DGND at single point

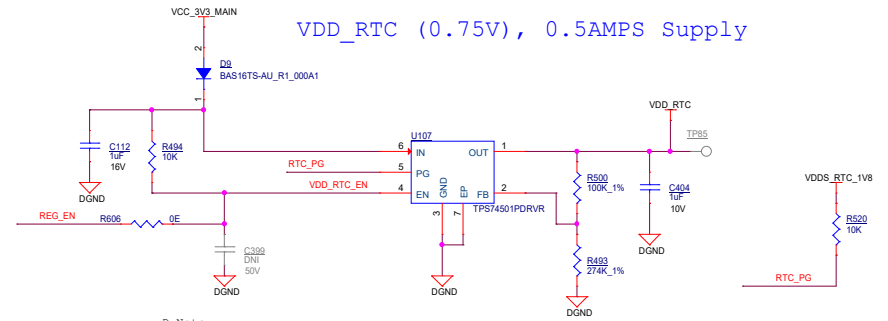


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## LOW POWER MODE CONFIGURATION

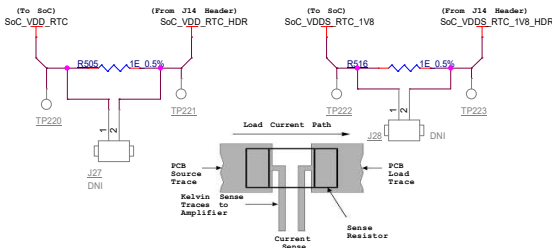


D-Note:-  
The enable pin of the discrete RTC supply (LDO) can be driven by the power-good signal of the regulator generating the main supply rail (VCC 3V3 MAIN). In case the regulator does not support a PG signal- output, a resistor pulled up to the LDO supply input can be used as EN input.



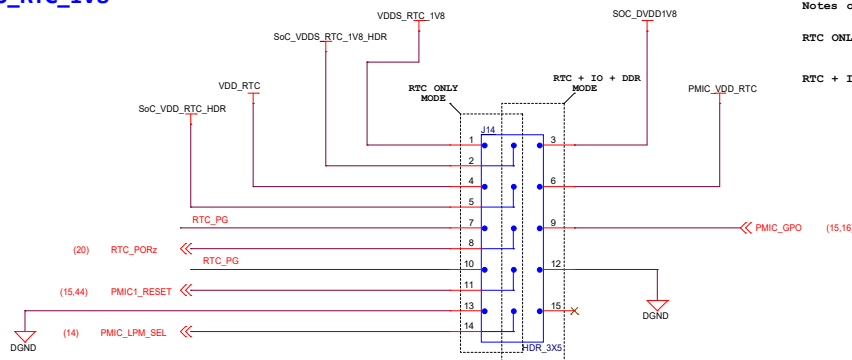
D-Note:-  
Adjust RTC PG pullup value to minimize the output slew.  
Keep the RTC PG to RTC PORz PCB trace short to minimize trace capacitance. Adjust the value of the external pullup resistor when an open-drain output PG is used as reset input to RTC PORz. The RTC PORz input has internal hysteresis and the internal reset could glitch when a slow rising input is applied. The slew rate is recommended to be faster than the limits specified in the LVC MOS IO buffer electrical specification to minimize possible noise coupling.

## CURRENT SENSE RESISTOR FOR SoC\_VDD\_RTC AND SoC\_VDDS\_RTC\_1V8



CAD NOTE:  
Follow Kelvin current sense routing for RTC supplies  
current sense resistor (R505 and R516). Follow the routing  
shown in the above figure that has been added as reference for  
kelvin current sense routing.

## RTC SUPPLY SELECTION



Note:  
Use 5x2 Female gang jumper to select the mode

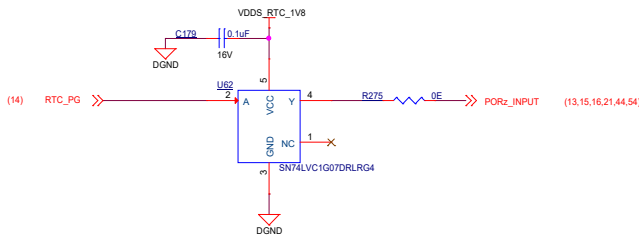
Notes on SoC\_VDD\_RTC and SoC\_VDDS\_RTC\_1V8 supply source:

**RTC ONLY MODE** - external discrete LDOs U113 (for SoC\_VDD\_RTC\_1V8) and U107 (for SoC\_VDD\_RTC) are used

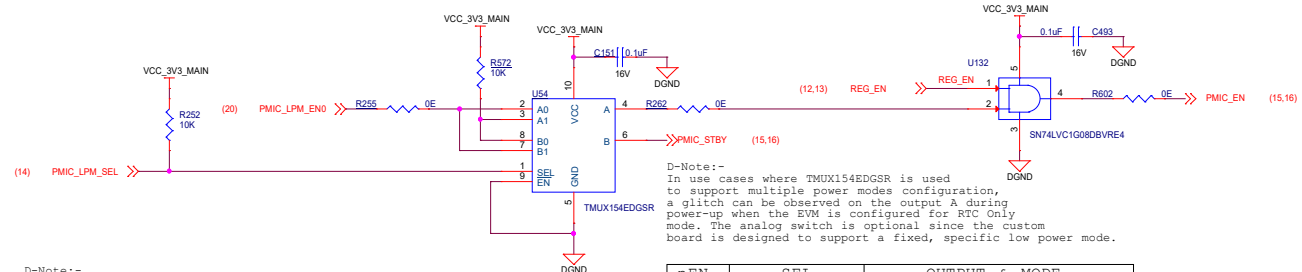
RTC + IO + DDR MODE - PMIC Buck2 (for SoC VDD5\_RTC 1V8) and  
LDO1 (in case of PMIC1 - TPS65215 is used) /  
LDO2 (in case of PMIC2 - TPS65214 is used)  
(for SoC VDD\_RTC are used

RTC Only MODE	TO SOC	RTC + IO + DDR MODE
VDD <sub>S_RTC_Iv8</sub>	SoC_VDD <sub>S_RTC_Iv8</sub>	SOC_VDD <sub>DIv8</sub>
VDD <sub>S_RTC</sub>	SoC_VDD <sub>S_RTC</sub>	PMIC_VDD <sub>S_RTC</sub>
RTC_PG	RTC_PORz	PMIC_GPO
RTC_PG	PMIC1_RESET (To PMIC 1)	DGND
DGND	PMIC_LPM_SEL	NC

## RTC\_PG TO PORz INPUT OPEN DRAIN BUFFER



## LOW POWER MODE TRIGGER SELECTION



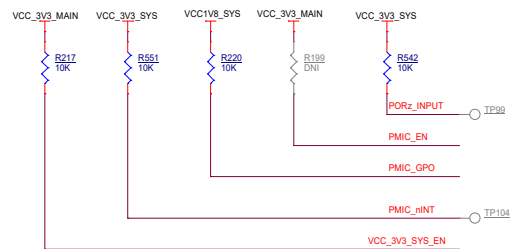
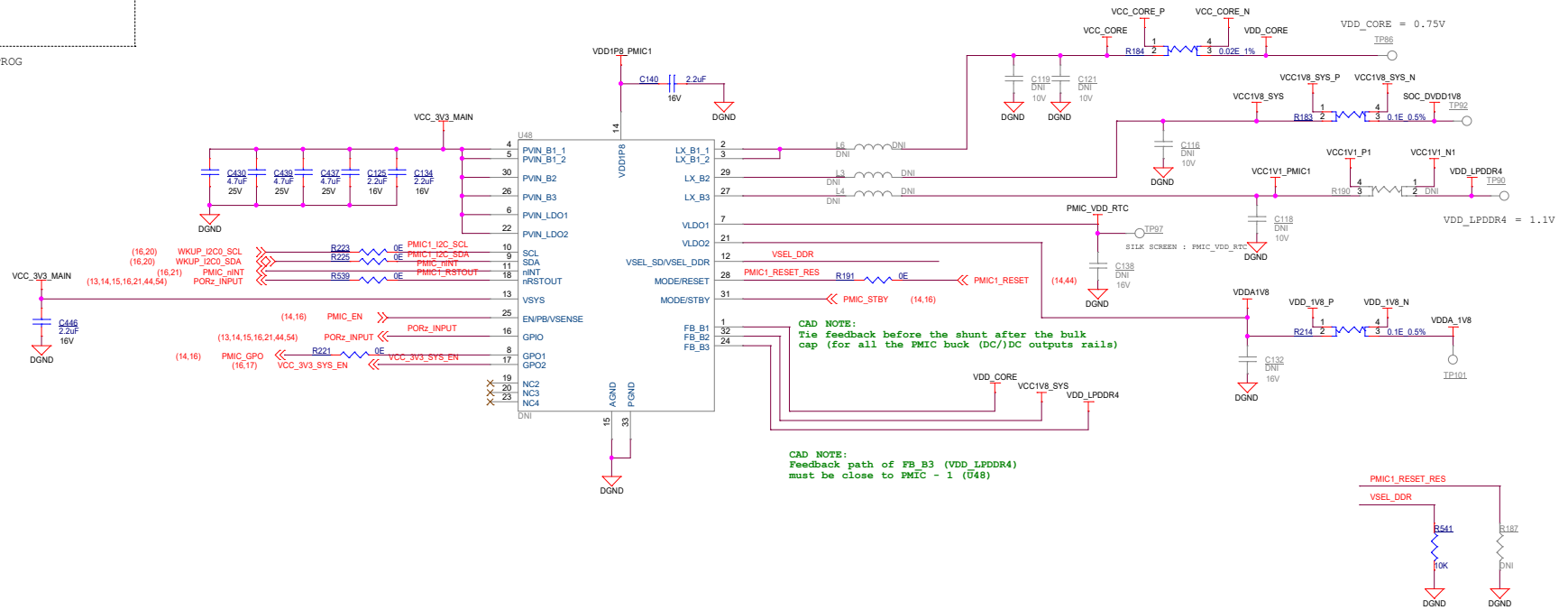
D-Note:-  
PMIC LPM SEL is generated based on 5x2 Female gang jumper configuration. By default the MUX SEL pin is high and PMIC LPM EN0 drives the PMIC STBY pin to turn-OFF the CORE and VDDA to support RTC + IO + DDR Mode. When the MUX SEL pin is low, the PMIC LPM EN0 drives the PMIC enable pin to support "RTC only". In this low power mode, the entire PMIC is turned-OFF and the RTC domain is supplied by external always-ON LDOs.

D-Note:- In use cases where TMUX154EDGSR is used to support multiple power modes configuration, a glitch can be observed on the output A during power-up when the EVM is configured for RTC Only mode. The analog switch is optional since the custom board is designed to support a fixed, specific low power mode.

nEN	SEL	OUTPUT & MODE	
L	L	A=A0 B=B0	RTC ONLY MODE
L	H (DEFAULT)	A=A1 B=B1	RTC + IO + DDR MODE



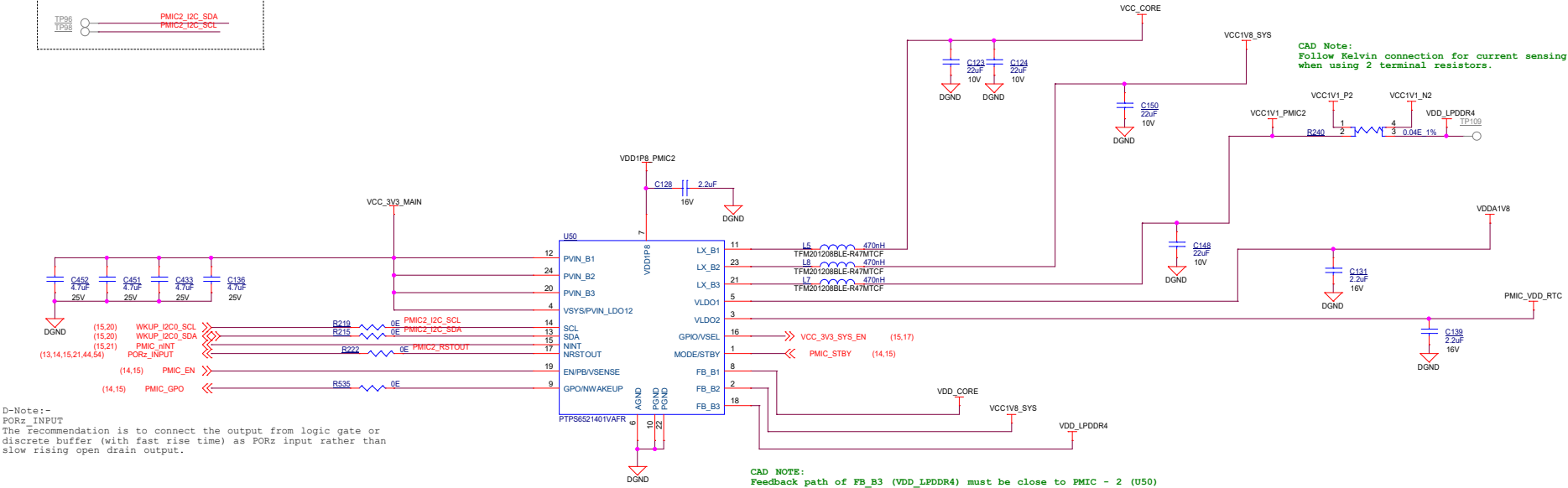
## COMMON PULL-UPS OF PMIC - 1 AND PMIC - 2



D-Note:-  
**PORZ\_INPUT**  
 When the PORZ input from the PMIC is connected directly to the PORZ input, adjust the RSTOUT2 pullup value to minimize the sleep. Keep the PCB trace short to minimize trace capacitance. Adjust the external pullup value when using an open-drain reset device. The reset delay time of the device should be as fast as recommended to be faster than the limit specified in the IO buffer electrical specification to minimize possible noise on the reset signal. The recommendation is to connect RSTOUT2 through a discrete Schmitt trigger push pull output buffer to the PORZ input of the processor. The PORZ input has internal pullup and the external reset could glitch when a slow rising input is applied.

SOC POWER SUPPLY PMIC - 2

PMIC 2 Config option



D-Note:-  
PORz\_INPUT  
The recommendation is to connect the output from logic gate or discrete buffer (with fast rise time) as PORz input rather than slow rising open drain output.

D-Note:-  
PORz inputs have slew rate requirements specified.  
When PMIC nRSTOUT is connected to PORz. Adjust the pull-up to minimize the rise time (100-200 ns) when using an open drain output. PORz is fail-safe and 3.3 V tolerant. The PORz input can be connected to 1.8 V or 3.3 V.

PROC181E1P1A

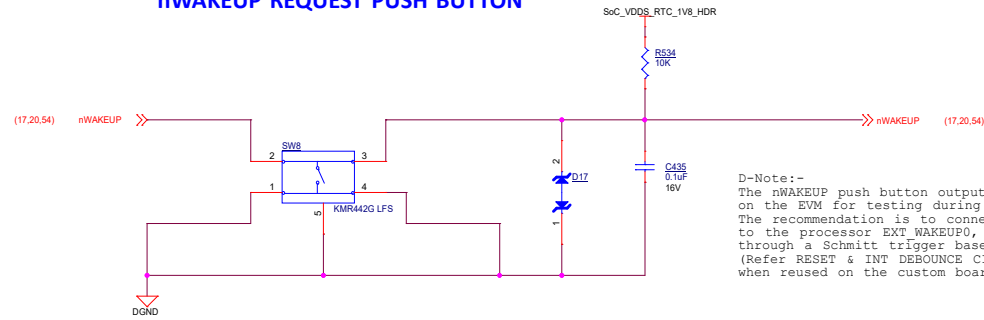
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Title SOC POWER SUPPLY PMIC - 2 (ALTERNATIVE)

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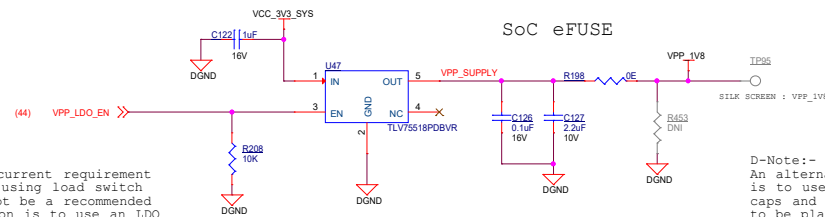
## nWAKEUP REQUEST PUSH BUTTON



## 1.8V VPP (eFUSE), 0.5AMPS SUPPLY

D-Note:-  
Alternate part suggestion  
TPSTA21-Q1, Automotive,  
500mA, low-noise ultra-low-IQ  
high-PSRR low-dropout (LDO)  
voltage regulator.

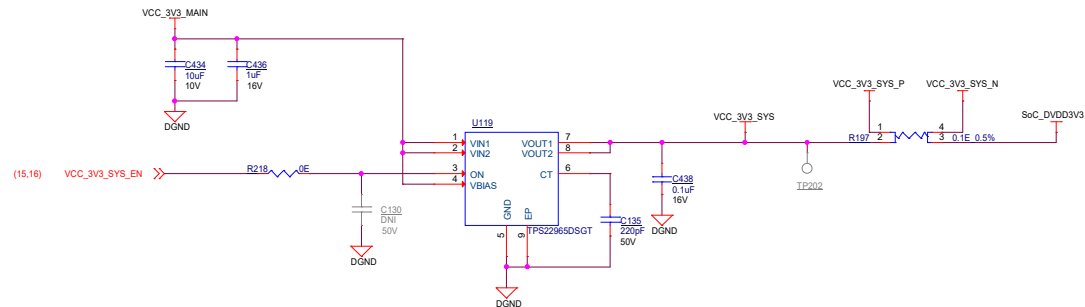
D-Note:-  
Okay to use VCC\_3V3\_MAIN



D-Note:-  
Given the transient load current requirement during eFuse programming, using load switch or FET based switch may not be a recommended approach. The recommendation is to use an LDO with fast load current transient response and quick output discharge that can be enabled by processor IO. A load switch or FET based switch is likely to have too much voltage drop (out of processor VPP supply ROC) that can't be compensated like when using an LDO.

D-Note:-  
An alternate way to source the VPP supply is to use an external supply. The recommended caps and discharge resistor are recommended to be placed near to the SOC VPP supply pin. One of the SOC GPIO output can be used to control the timing of the external power supply output.

## VCC\_3V3\_SYS LOAD SWITCH



PROC181E1PIA

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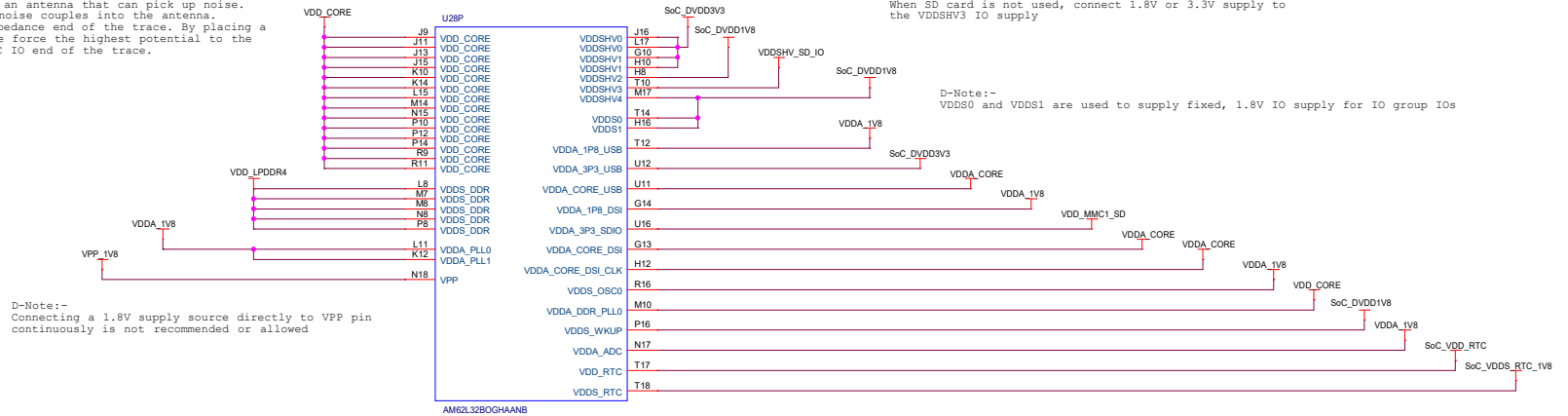


Title nWAKEUP PUSH BUTTON, LOAD SWITCH AND VPP LDO

Size	PROC181E1-1A	Rev
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# SOC POWER SUPPLIES AND SUPPLY RAILS

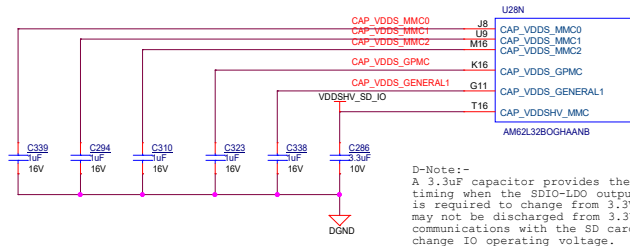
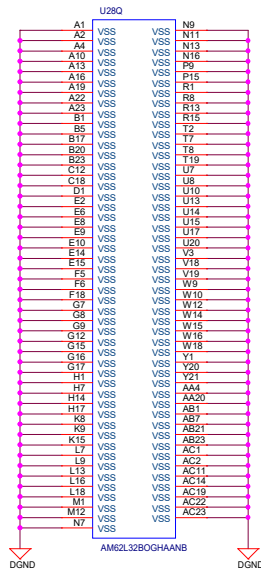
D-Note:-  
A Trace connected to SOC pad (IO) is effectively an antenna that can pick up noise. A potential will be generated on the trace when noise couples into the antenna. This potential will be largest on the highest impedance end of the trace. By placing a pull-up or pull-down near the SoC pin (input), we force the highest potential to the open-circuit end of the trace rather than the SoC IO end of the trace.



D-Note:-  
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

D-Note:-  
Common SOC LVCMOS IO interface guidelines  
1. Most of the SOC IOs are not fail-safe. No input should be applied before SOC supplies ramps.  
2. SOC LVCMOS inputs have minimum slew rate requirements specified  
3. SOC IO buffers are off during Reset and after Reset. A pull is required in case SOC IOs or the attached device inputs could float.  
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull.  
When adding pull is not feasible, ensure the traces are routed away from noisy signals

## SOC VSS



D-Note:-  
Select capacitor with ESR < 1 ohm  
Ensure the PCB loop inductance is < 2.5 nH  
Select 0201 package or smallest possible package nearest to 0201  
Refer SOC Data sheet

PROC181E11A

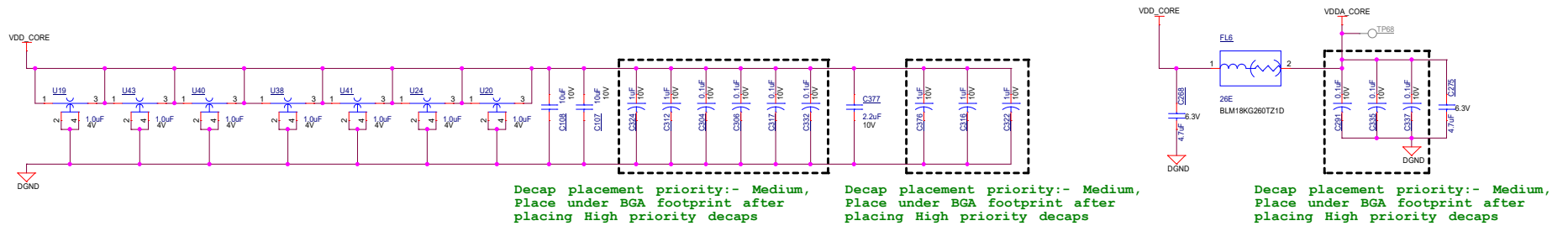
Designed for TI by Mistral Solutions Pvt Ltd



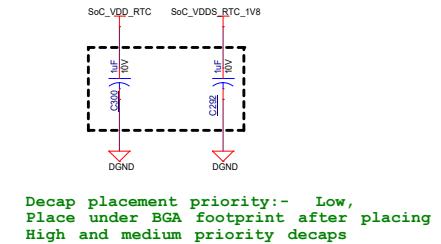
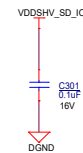
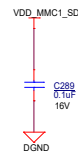
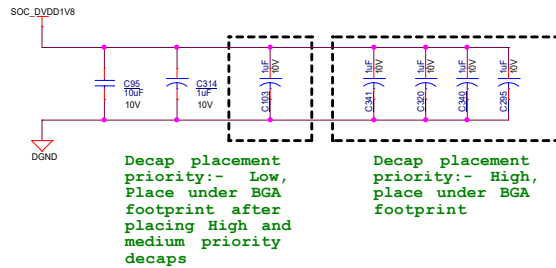
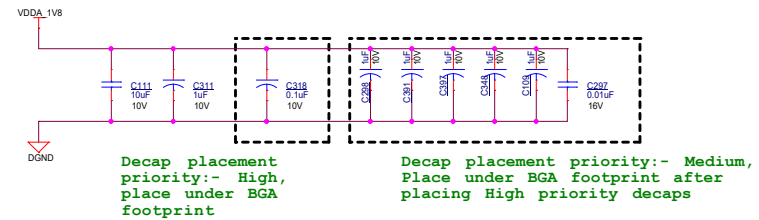
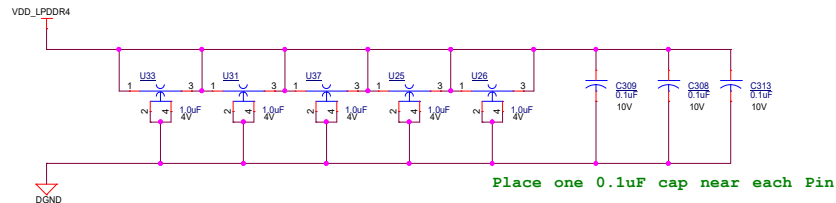
Title SOC POWER SUPPLIES, SUPPLY RAILS AND SOC GROUND VSS

Size	PROC181E1-1A	Rev	E1-1A
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# SOC POWER SUPPLIES - DECAPS



Place one 0.1uF cap near each Pin



R-Note:-  
Use of 3 terminal caps optimizes use of bulk caps quantity and minimizes the PCB loop inductance

PROC181E1PIA

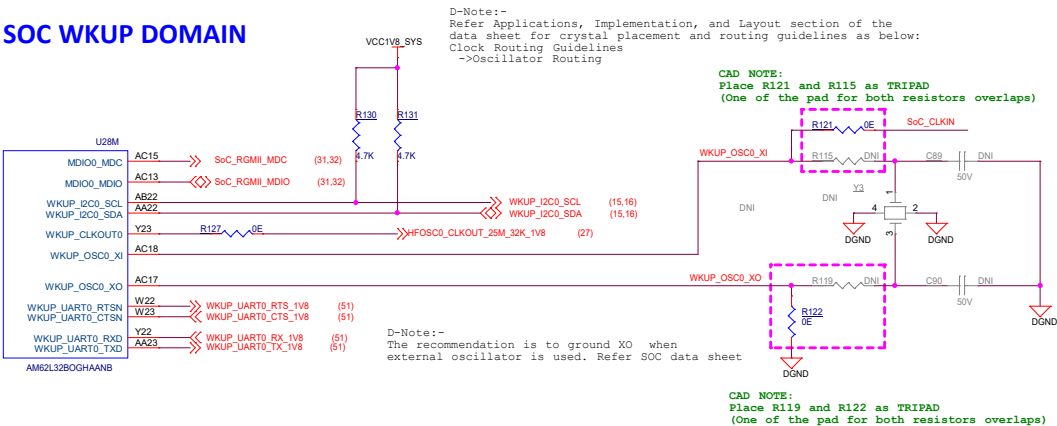
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Title SOC POWER SUPPLIES - DECAPS

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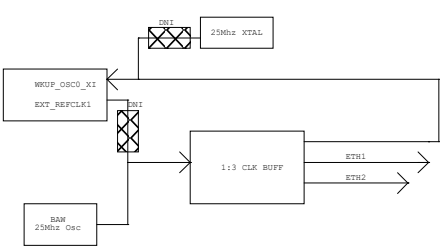
SOC WKUP DOMAIN



D-Note:-  
The processor performance has been validated only with a 25 MHz Crystal/clock source connected to WKUP\_OSC0 (25 MHz is the only clock frequency supported). The data sheet shows WKUP\_OSC0 not starting until after the core voltage because there are some cases where the oscillator may not start until VDD\_CORE is valid. In most cases the oscillator will start as early as VDD\_OSC0, but this may not always be the case. This diagram in the data sheet is showing the maximum start-up time, which must include the case where the delay is based on VDD\_CORE being valid.

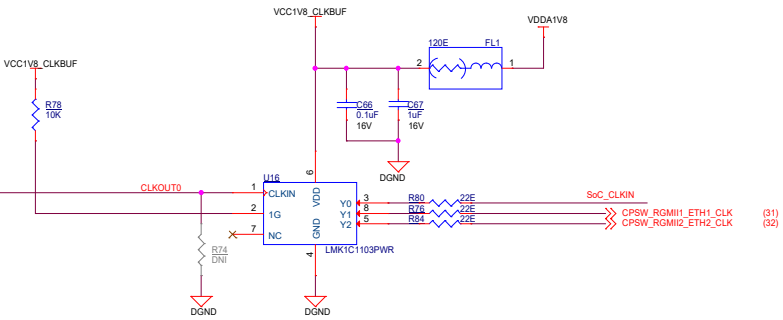
D-Note:-  
The recommendation is to connect the 25 MHz crystal directly to the SOC XI and XO pins (no series or parallel resistors are recommended). The internal oscillator implements AGC (Automatic Gain Control) for amplitude control. The recommendation is to match the SOC crystal and the EPHY crystal specifications

OSCILLATOR



D-Note:-  
SOC data sheet section for LVCMOS specifications:  
WKUP\_OSC0 LVCMOS Digital Clock Source Requirements  
Match the SOC and the EPHY clock specs

SOC & ETHERNET PHY CLOCK BUFFER

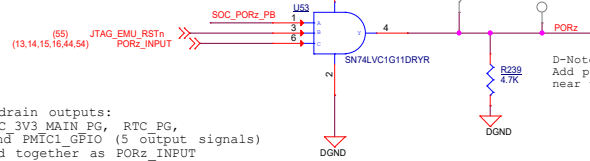




# SOC RESET

## POWER ON RESET

D-Note:-  
Place the pullup for PORz\_INPUT  
near to the ANDing logic AND gate input

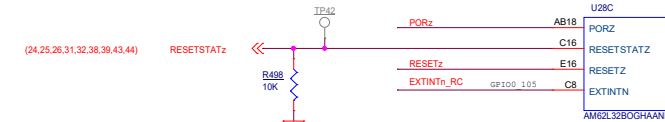


D-Note:-  
Not connecting a valid PORz input could  
cause unpredictable and probably random  
behaviour, since the processor is not getting  
a valid reset, internal circuits could be in  
random states. Slow rising reset signal could  
cause glitches internal to the SOC reset circuit.  
Use of discrete buffer and having the fast rising  
output of the buffer drive the PORz is recommended

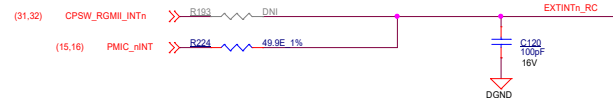
D-Note:-  
Add provision for 22pF glitch filter  
near to the SOC PORz input pin

D-Note:-  
PORz input is 3.3V tolerant.  
PORz ANDing logic AND gate supply is connected  
to VCC\_3V3\_SYS. This is within the PORz fail-safe  
input range.

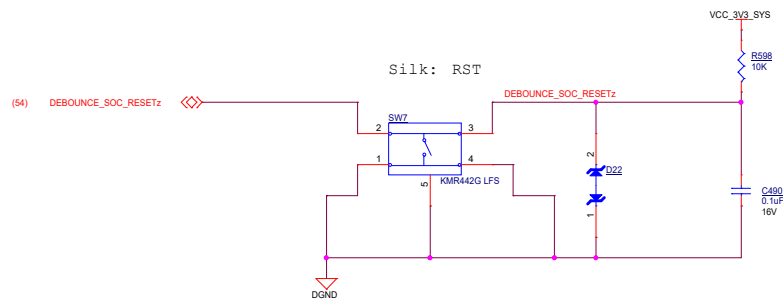
## SOC - RESET



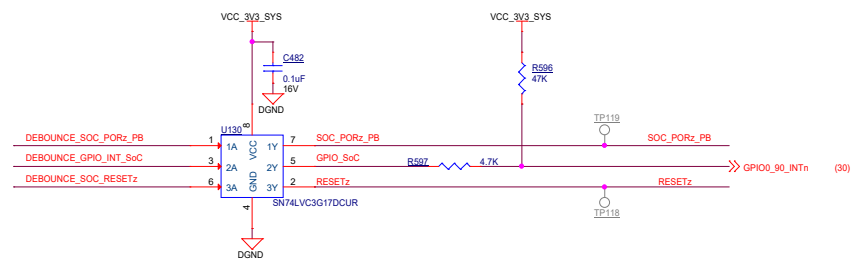
D-Note:-  
Open drain output type IO EXTINTn  
has slow rate limit specified when  
pulled to 3.3V supply. An RC is  
recommended at the input.  
Refer TMS64EVM.



## SOC WARM RESETz PUSH BUTTON

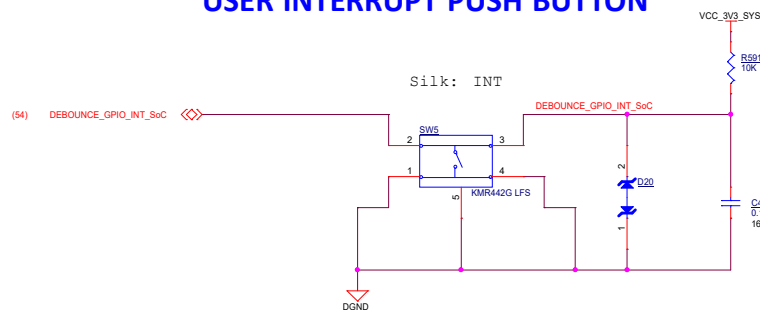


## RESET & INT DEBOUNCE CIRCUIT

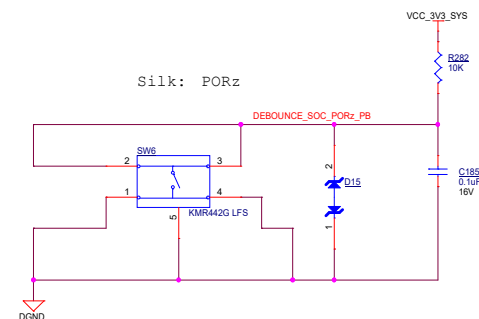


Processor LVCMOS I/Os (inputs) have slow rate requirement specified.  
A Schmitt trigger based debouncing logic is recommended for the slow ramp pushbutton output (+ RC)  
connected to the processor warm reset inputs.  
Debouncing logic is recommended when push button + RC or RC is used at the LVCMOS inputs.

## USER INTERRUPT PUSH BUTTON



## SOC PORz RESET PUSH BUTTON



PROC181E1A

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Title SOC RESET

Size PROC181E1-1A

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Rev E1-1A

# BOOT MODE SWITCHES

D-NOTE:-

The device supports the following BOOTMODE pin mapping options:

1. Reduced Pincount - Using only 4 of the bootstrap pins BOOTMODE[15:12]
2. Full Pincount - Using all 16 of the bootstrap pins BOOTMODE[15:0]
3. Configuring the reduced pincount bootmode resistors to boot from eFuse

## FULL PINCOUNT SWITCHES

D-Note:-

To reduce the number of resistors used for bootmode configuration (pullup/pulldown) when using reduced pin count bootmode, the input buffers for BOOTMODE[11:0] inputs (pins) are disabled during POR (cold reset) unless BOOTMODE[15:14] are configured as '00' (Full pincount bootmode).

D-Note:-  
VCC3V3\_TA supply is used for bootmode configuration to support test automation. The recommendation is to connect to SoC\_DVDD3V3 on the custom board design when test automation or bootmode buffers are not used.

SWITCH ON = LOGIC 1  
SWITCH OFF = LOGIC 0

Silk: BMODE 0-7

(43) SYS\_BOOTMODE0  
(43) SYS\_BOOTMODE1  
(43) SYS\_BOOTMODE2  
(43) SYS\_BOOTMODE3  
(43) SYS\_BOOTMODE4  
(43) SYS\_BOOTMODE5  
(43) SYS\_BOOTMODE6  
(43) SYS\_BOOTMODE7

D-Note:-  
When dip switches are used on custom board, an external ESD protection may be required if the DIP switches are expected to be configured in an uncontrolled ESD environment

D-Note:-  
When DIP switches are used, reduce the resistor values used for the divider to 47K and 470R maintaining the ratio (for improved noise performance)

### BOOTMODE PINS

Signals from Bootmode buffer

(43) BOOTMODE10  
(43) BOOTMODE1  
(43) BOOTMODE0  
(43) BOOTMODE4  
(43) BOOTMODE2  
(43) BOOTMODE3  
(43) BOOTMODE7  
(43) BOOTMODE6  
(43) BOOTMODE5  
(43) BOOTMODE8  
(43) BOOTMODE11

RA1 1 8 1K  
2 7  
3 6  
4 5  
RA2 1 8 1K  
2 7  
3 6  
4 5  
RA4 1 8 1K  
2 7  
3 6  
4 5

SoC\_VOUT0\_DATA10 (28.37)  
SoC\_VOUT0\_DATA1 (28.37)  
SoC\_VOUT0\_DATA0 (28.37)  
SoC\_VOUT0\_DATA4 (28.37)  
SoC\_VOUT0\_DATA2 (28.37)  
SoC\_VOUT0\_DATA3 (28.37)  
SoC\_VOUT0\_DATA7 (28.37)  
SoC\_VOUT0\_DATA6 (28.37)  
SoC\_VOUT0\_DATA5 (28.37)  
SoC\_VOUT0\_DATA8 (28.37)  
SoC\_VOUT0\_DATA9 (28.37)  
SoC\_VOUT0\_DATA11 (28.37)

D-Note:-  
Connect SYS\_BOOTMODE signals when bootmode buffers are not used

D-NOTE:-

1. 1K Resistor at the output of the buffer is recommended
2. Replace 1K Resistor at the output of the buffer with resistor of value 0E when bootmode buffers are not used

### BOOT MODES SUPPORTED

1. eMMC
2. OSPI
3. MMC1 - uSD Card
4. UART
5. USB0 DFU
6. USB0 MS

## FAQs FOR BOOTMODE CONFIGURATION (WITH BUFFER OR WITHOUT BUFFER)

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1391522/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am62l---bootmode-implementation-without-buffers>

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1414148/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am62l---bootmode-implementation-with-buffers>

D-Note:-

Boot from eFuse can be configured using the reduced pin count bootmode configuration.

## REDUCED PINCOUNT SWITCH

SWITCH ON = LOGIC 1  
SWITCH OFF = LOGIC 0

Silk: BMODE 12-15

(43) SYS\_BOOTMODE12  
(43) SYS\_BOOTMODE13  
(43) SYS\_BOOTMODE14  
(43) SYS\_BOOTMODE15

### BOOTMODE PINS

Signals from Bootmode buffer

(43) BOOTMODE12  
(43) BOOTMODE13  
(43) BOOTMODE14  
(43) BOOTMODE15

RA3 1 8 1K  
2 7  
3 6  
4 5

SoC\_VOUT0\_DATA12 (28.37)  
SoC\_VOUT0\_DATA13 (28.37)  
SoC\_VOUT0\_DATA14 (28.37)  
SoC\_VOUT0\_DATA15 (28.37)

D-Note:-  
Connect SYS\_BOOTMODE signals when bootmode buffers are not used

D-NOTE:-

1. 1K Resistor at the output of the buffer is recommended
2. Replace 1K Resistor at the output of the buffer with resistor of value 0E when bootmode buffers are not used

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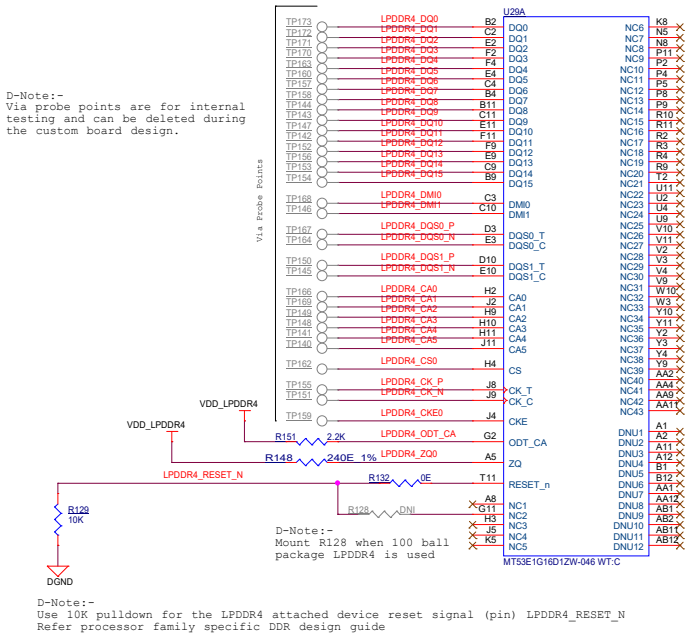


Title BOOT MODE CONFIGURATION RESISTORS AND DIP SWITCHES

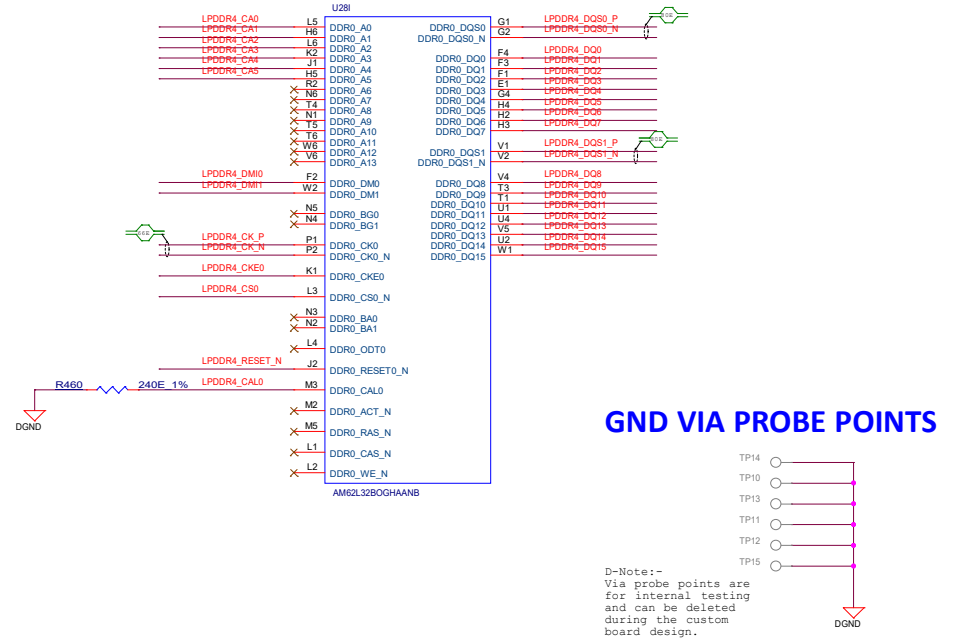
Size	PROC181E1-1A	Rev	E1-1A
C			
Date:	Monday, October 06, 2025	Sheet	22 of 56

## LPDDR4 DEVICE

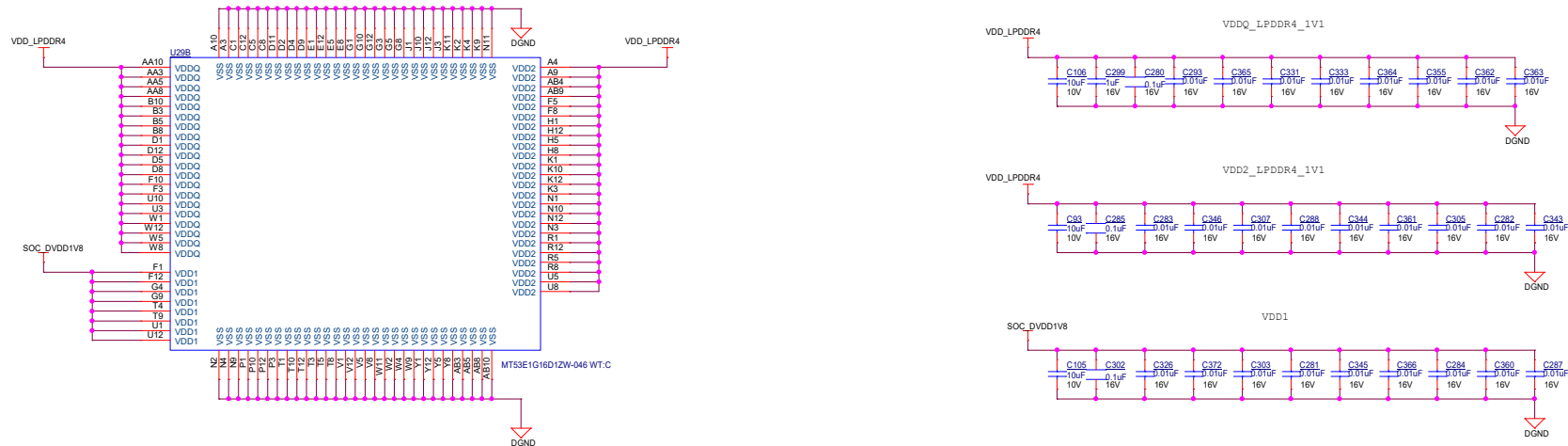
Silk: LPDDR4



## SOC LPDDR4 INTERFACE



## LPDDR4 POWER DECAPS



PROC181E1P1A

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Title	SoC DDRSS AND LPDDR4 DEVICE INTERFACE
-------	---------------------------------------

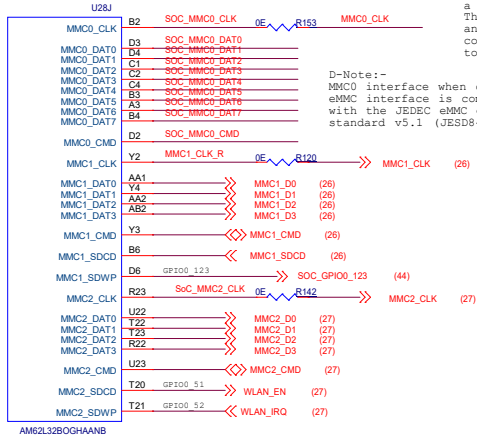
Size	PROC181E1-1A	Rev
C		E1-1A
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# eMMC INTERFACE

## SOC - MMC Interface

D-Note:-  
Series resistor (0E) provision on MMC0\_CLK is recommended to control reflections (for addressing signal integrity related concerns)



D-Note:-  
The processor family implements a soft PHY for eMMC interface. The pulls required for DQ, Clock and other eMMC interface control signals are recommended to be implemented externally

D-Note:-  
MMC0 interface when configured for eMMC interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)

D-Note:-  
The processor I/Os associated with the MMC0 port will be turned off until software initializes them. This means any signals without internal pulls will be floating until software boots and initializes the I/Os. The JEDEC eMMC electrical standard v5.1 (JESD84-B51) requires the eMMC device to have internal pulls on the DAT[7:1] pins, but the other pins do not have internal pulls. We recommend external pull-ups on the CMD and DAT0 signals and an external pull-down on the CLK signal. The eMMC standard also says 10k pull-ups are the min value, so we do not recommend using a 10k resistor because it may be less than 10k. We typically recommend using 47k resistors to minimize loading on the signals since the pulls are only used to hold the signals in a valid logic state when not driven.

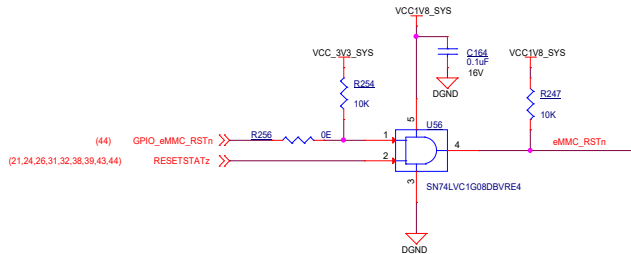
D-Note:-  
Ensure eMMC\_RSTn (RST\_N) pin function (Reset input) has been enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional

R-Note:-  
What is the reason we selected pulldown instead of pullup for eMMC, SD card or other peripherals? Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

D-Note:-  
Use case for GPIO input to the ANDing logic :  
The GPIO reset option makes it possible for software to reset the attached device (eMMC or SPI or SD card or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

D-Note:-  
Use case for ANDing logic :  
You could eliminate the GPIO option and only use the reset output (Warm), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.

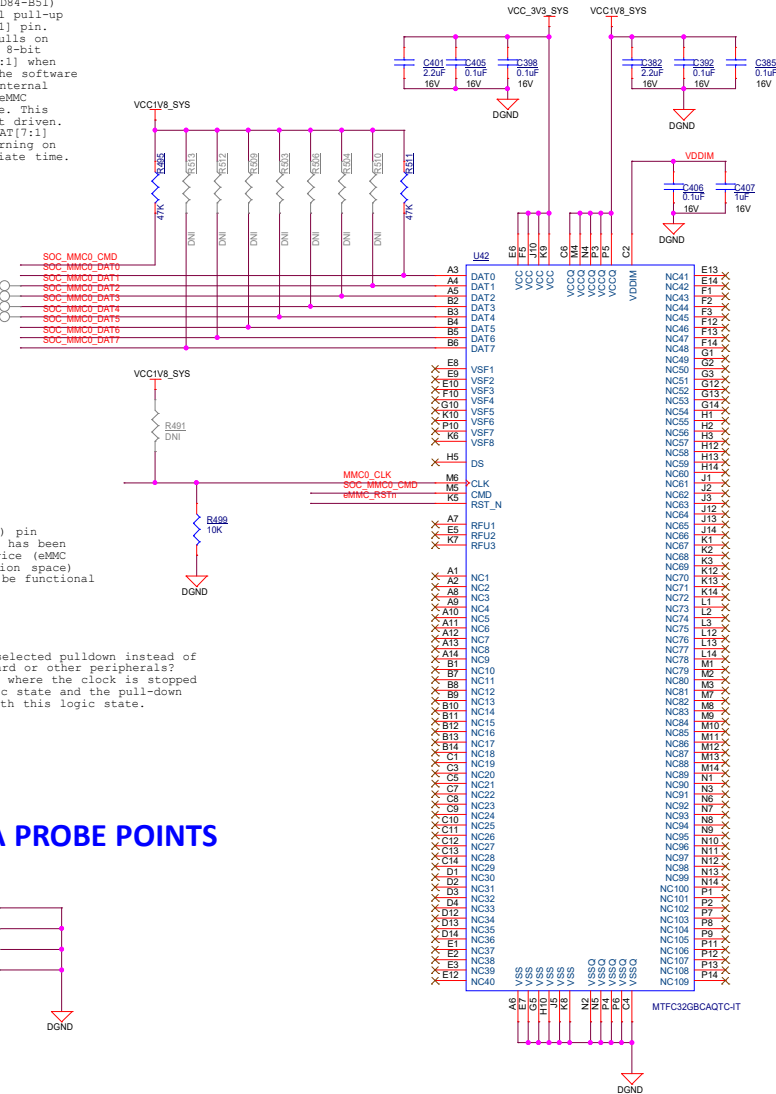
## eMMC FLASH RESET



D-Note:-  
In case ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider could be used alternatively for level translation, provided optimum impedance value of the resistor divider is selected. If too high value is used for the resistors, the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If resistor value used is too low it will cause the AM62Lx to source too much steady-state current during normal operation.

D-Note:-  
ANDing logic additionally performs level translation. Verify the Reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch could cause supply leakage and affect PMIC (SOC) operation

## eMMC FLASH



## GND VIA PROBE POINTS



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Title SOC MMC[0:2] INTERFACE AND eMMC FLASH + RESET

Size PROC181E1-1A

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Date: Monday, October 06, 2025

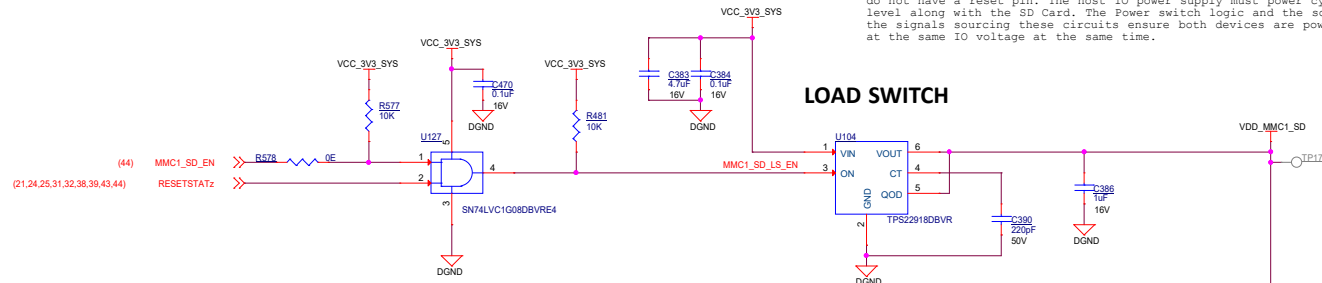
Rev

E1-1A

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## SD CARD INTERFACE

## SD CARD RESET

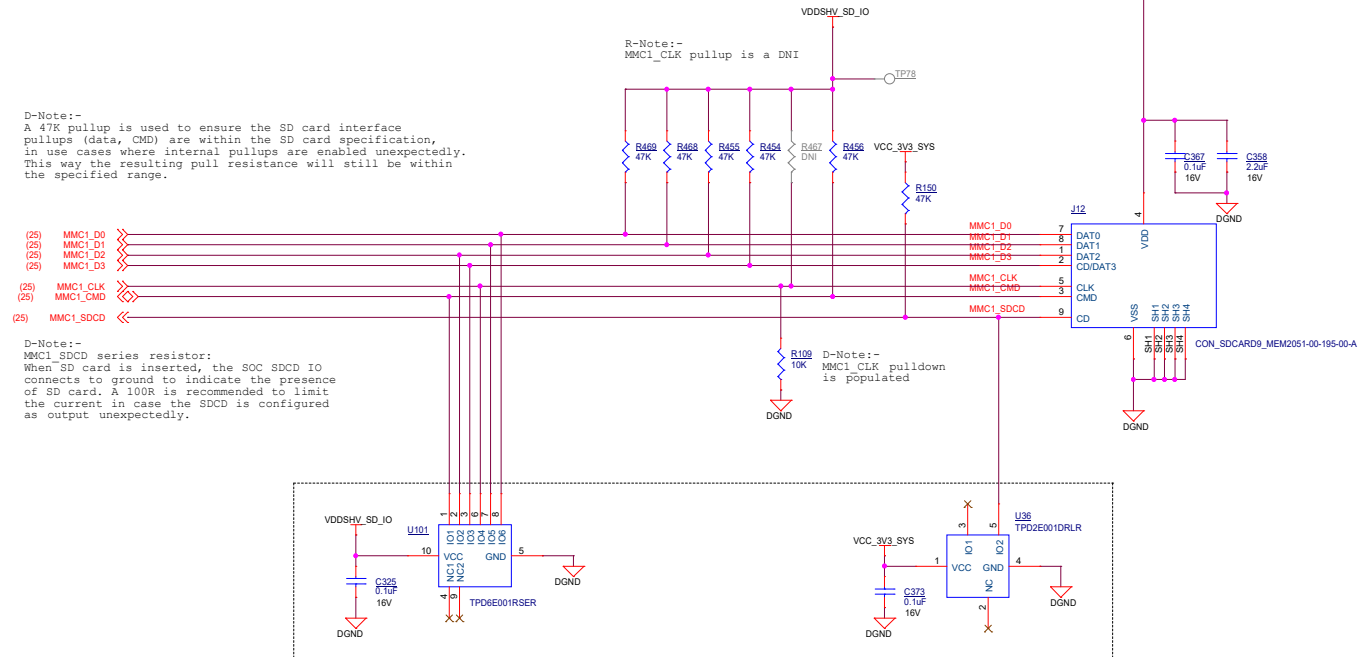


## LOAD SWITCH

D-Note:-  
TO support UHS-I SD Card interface, the pullups are recommended to be connected to the 3.3V/1.8V switched LDO output (can be the integrated LDO output).

R-Note:-  
MMC1\_CLK pullup is a DNI

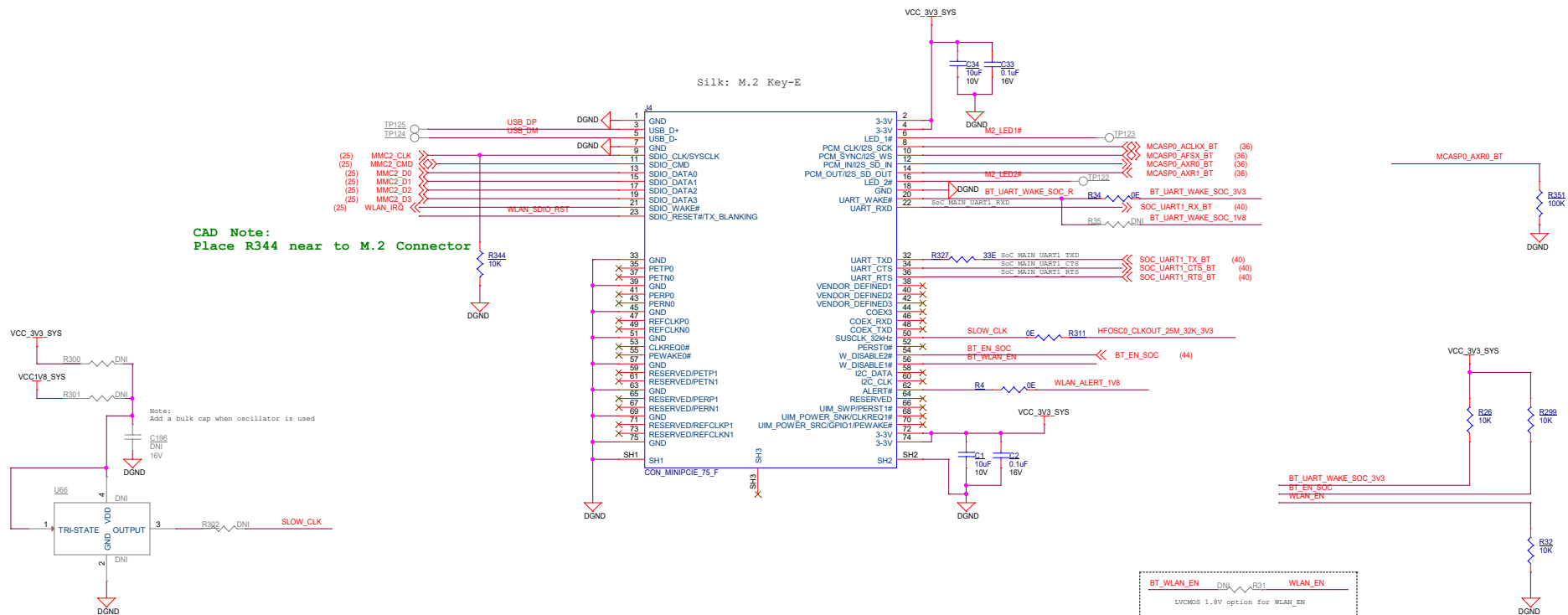
D-Note:-  
A 47k pullup is used to ensure the SD card interface pullups (data, CMD) are within the SD card specification, in use cases where internal pullups are enabled unexpectedly. This way the resulting pull resistance will still be within the specified range.



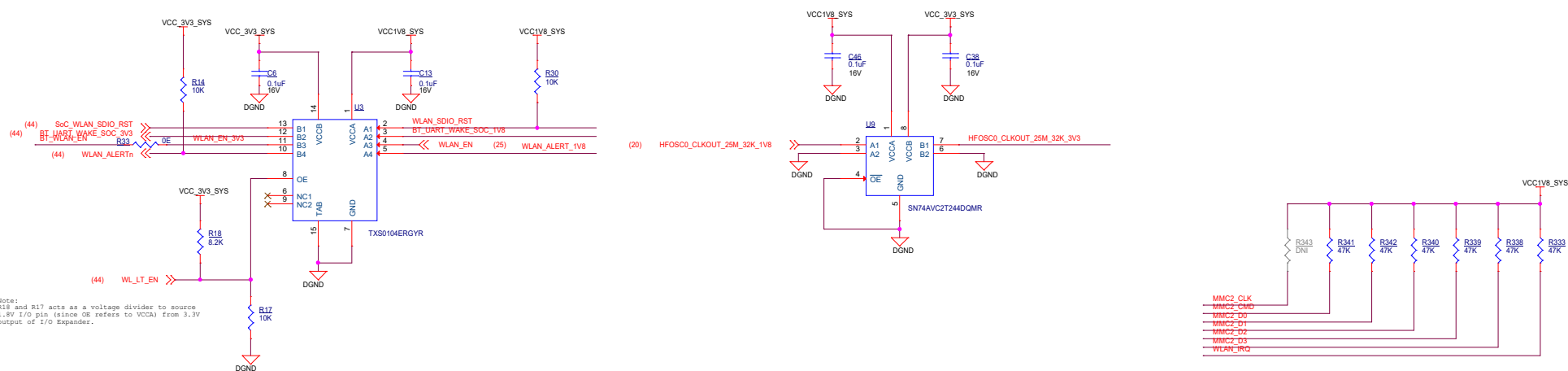
CAD Note:  
Place external ESD protection  
near to SD Card Connector



## M.2 INTERFACE - SDIO



## M.2 LEVEL TRANSLATORS



PROC181E1P1A

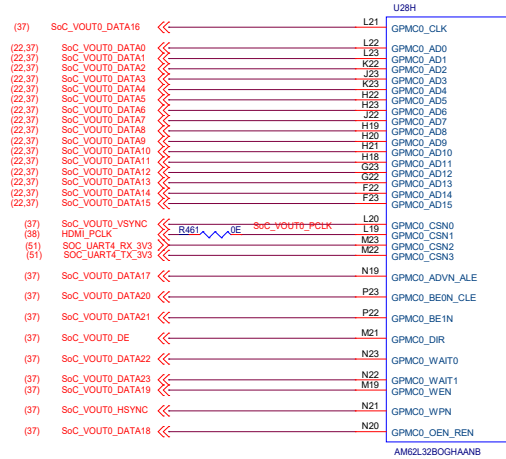
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Title				M.2 INTERFACE AND CONNECTOR			
Size		PROC181E1-1A				Rev	
C						E1-1A	
Date:		Monday, October 06, 2025		Sheet		27 of 56	

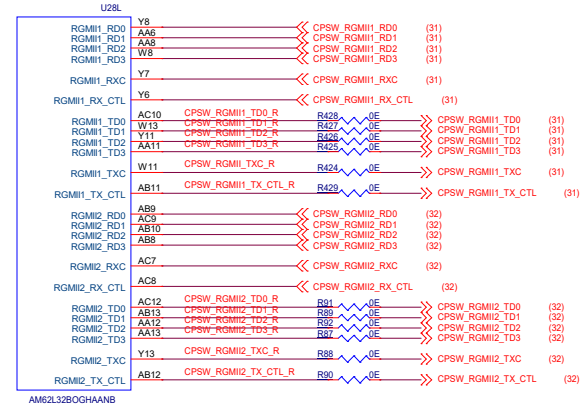
D-Note:-  
Shorting of multiple bootmode inputs together is not recommended or allowed, since the bootmode inputs have alternate functions that could be configured after boot (can be set as outputs). Shorting the bootmode pins directly to VCC or ground directly is not recommended. Connect each of the bootmode pins through separate resistor. Choose the bootmode resistor value based on the use case (10K or similar)

## SOC - GPMC



## SOC - ETHERNET INTERFACE

D-Note:-  
The Ethernet interface (CPSW3G)  
interface supports 1.8V IO level only



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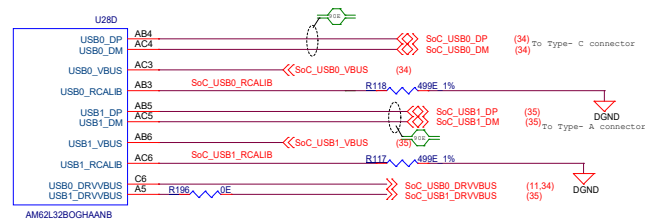


Title SOC PERIPHERALS 1 - GPMC AND CPSW3G ETHERNET INTERFACE

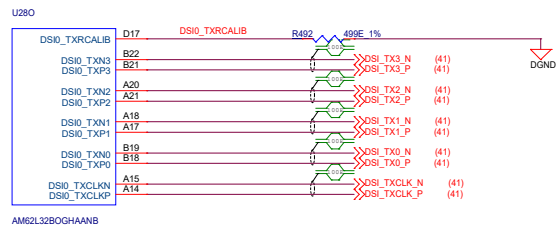
Size PROC181E1-1A Rev E1-1A

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SOC - USB



SOC - DSI



PROC181E1P1A

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Title SOC PERIPHERALS 2 - USB AND DSI INTERFACE

Size PROC181E1-1A

C

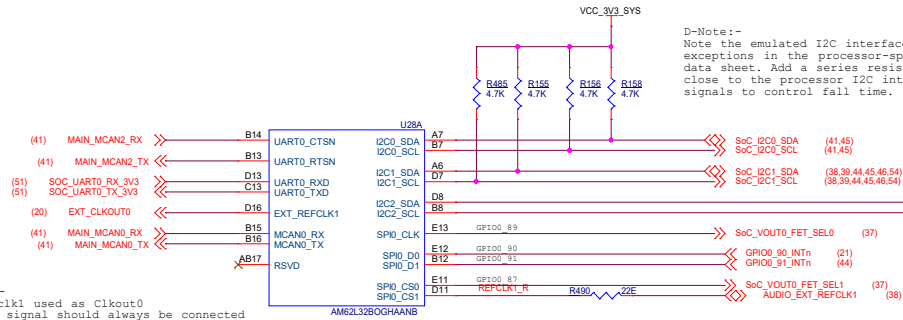
Date: Monday, October 06, 2025

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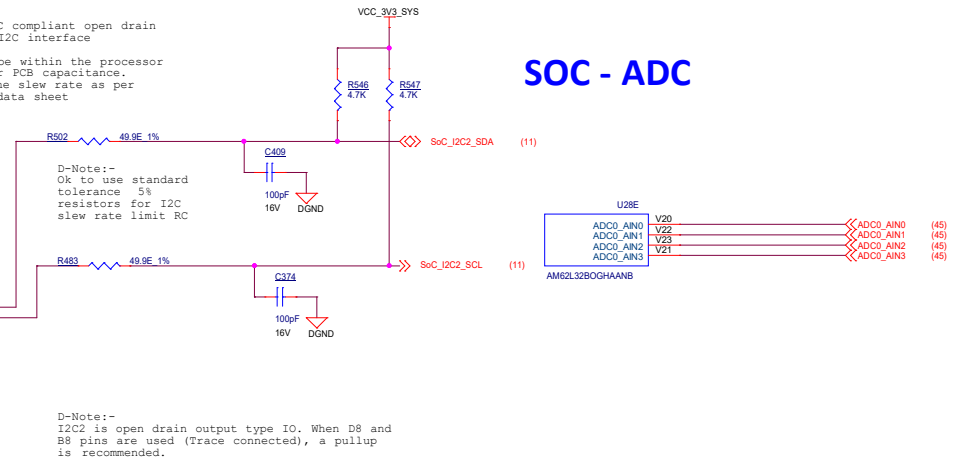
of 56

Rev E1-1A

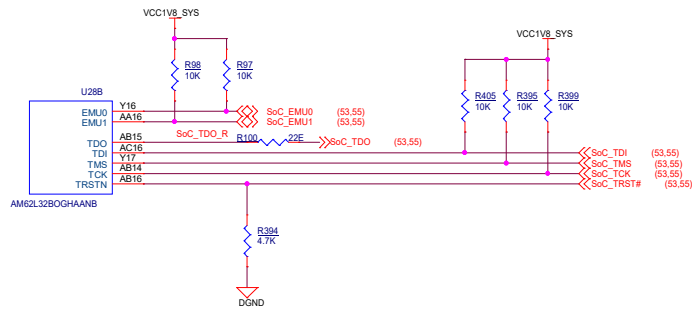
## SOC - UART, MCAN , I2C and IOs



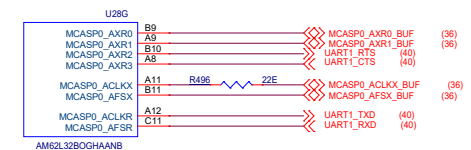
## SOC - ADC



## SOC- JTAG



## SOC - MCASP and UART



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Title  
SOC PERIPHERALS 3 - McASP, UART, SPI, I2C, MCAN, JTAG, ADC INTERFACE

Size  
PROC181E1-1A

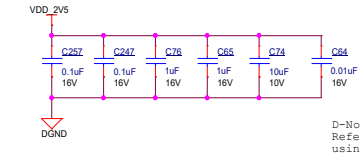
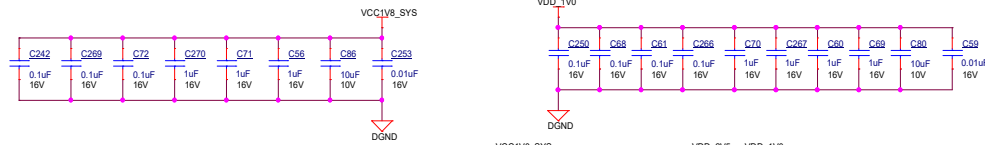
C  
Date: Monday, October 06, 2025

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E1-1A

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# CPSW3G RGMII\_1 ETHERNET PHY

D-Note:-  
The caps and values used are as per the EPHY datasheet recommendations.

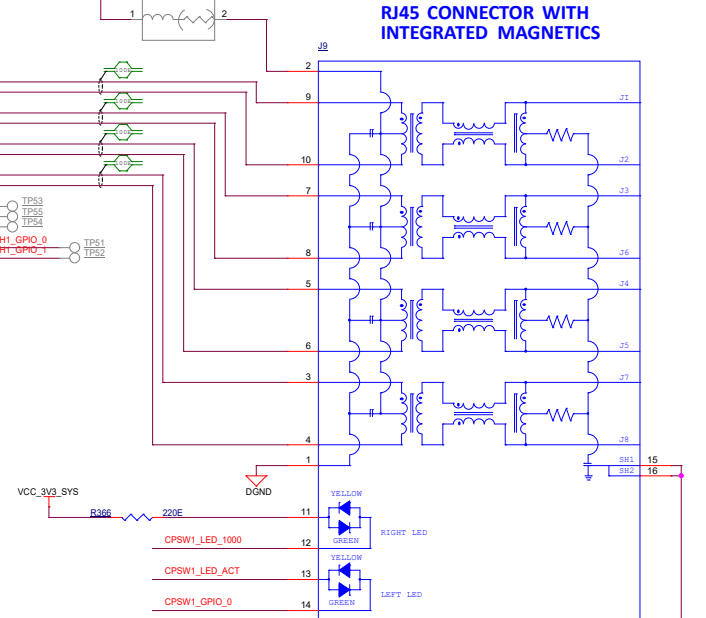


D-Note:-  
Refer to DP83867ERGZ-R-EVM when using LAN Discrete Transformer Module and RJ45 connector

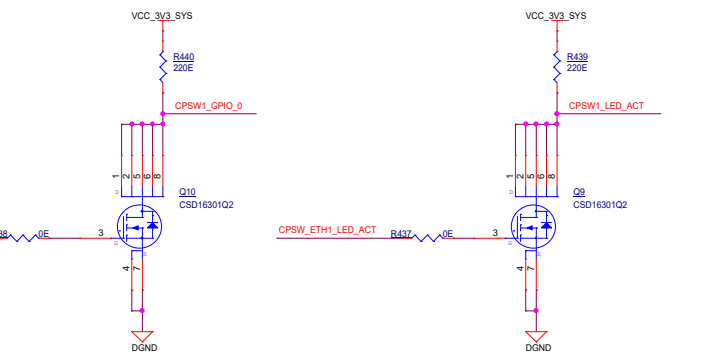
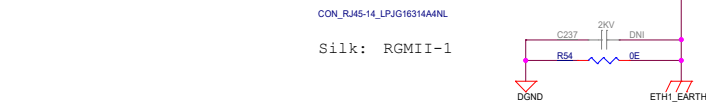
D-Note:-  
Verify the EPHY power sequence requirements for Two-Supply Configuration and optionally Three-Supply Configuration when 1.8V supply is connected to VDDA1P8

R-Note:-  
Ferrite is DNI

## RJ45 CONNECTOR WITH INTEGRATED MAGNETICS



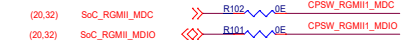
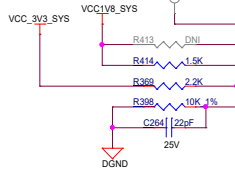
Silk: RGMII-1



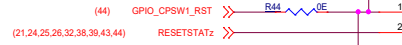
D-Note:-  
DP83867 EPHY clock input amplitude Recommended XI clock input amplitude is 1.8V irrespective of the EPHY IO supply. A CAPACITOR DIVIDER is recommended when the clock amplitude is 3.3V

D-Note:-  
Refer EPHY EVM for JTAG connection

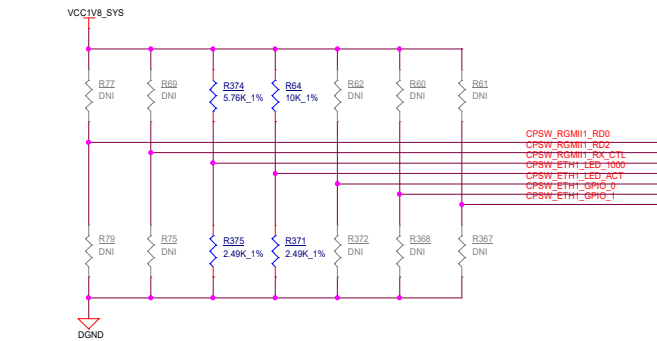
CAD NOTE:  
TP58 is a via probe point



R-Note:-  
Pullup is enabled for SOC GPIO input



R-Note:-  
Verify the resistor mounting configuration for resistors that are marked as DNI



# CPSW3G RGMII\_2 ETHERNET PHY

D-Note:-  
The caps and values used are as per the EPHY data sheet recommendations.

D-Note:-  
Refer to DP83867ERG2-R-EVM when using LAN Discrete Transformer Module and RJ45 connector

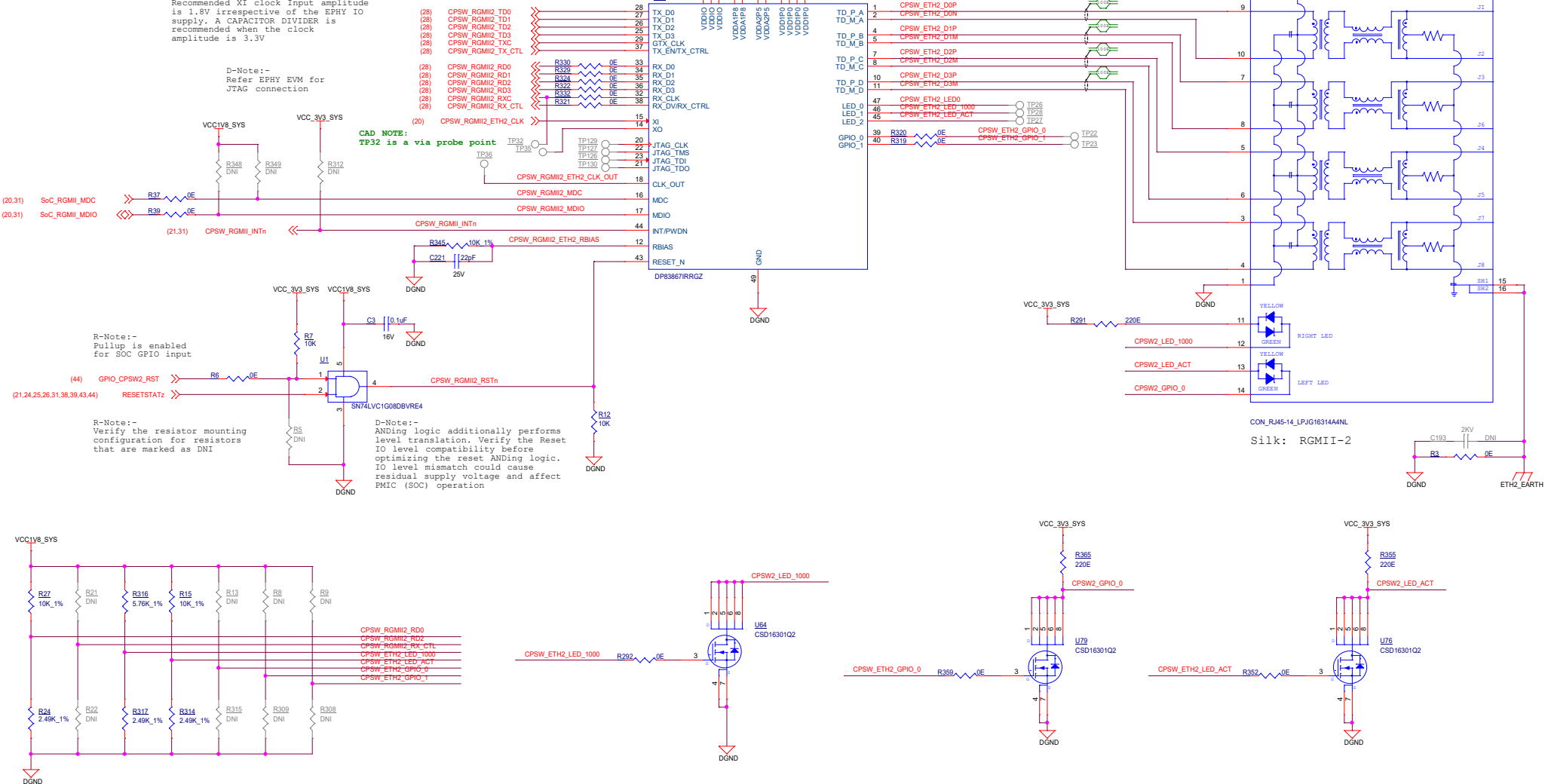
## RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

D-Note:-  
DP83867 EPHY clock input amplitude Recommended XI clock input amplitude is 1.8V irrespective of the EPHY IO supply. A CAPACITOR DIVIDER is recommended when the clock amplitude is 3.3V

D-Note:-  
Refer EPHY EVM for JTAG connection

D-Note:-  
Verify the EPHY power sequence requirements for Two-Supply Configuration and optionally Three-Supply Configuration when 1.8V supply is connected to VDDA1P8

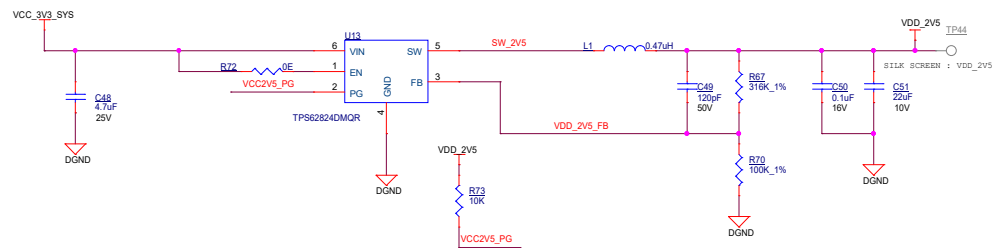
R-Note:-  
Ferrite is DNI



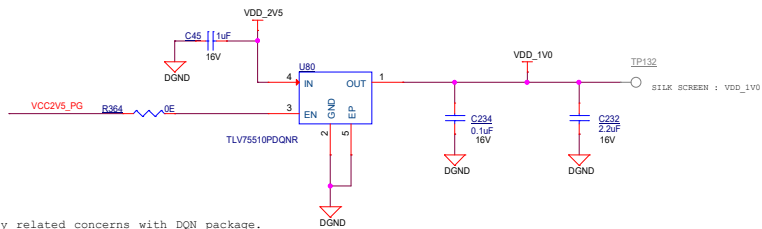


POWER SUPPLY (CORE) FOR ETHERNET PHY

2.5V (ETHERNET PHY), 1.0AMPS SUPPLY

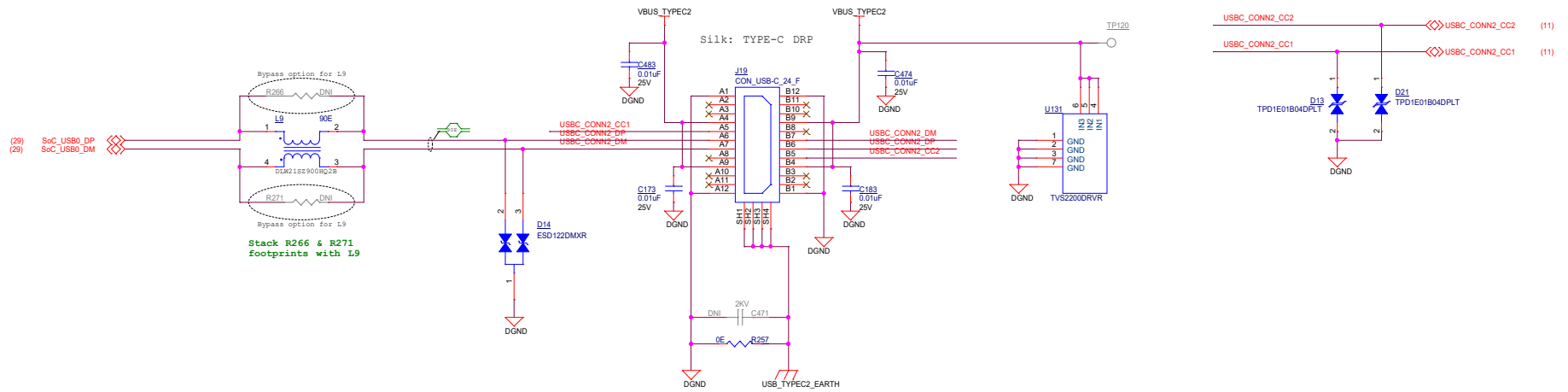


1.0V (ETHERNET PHY), 0.5AMPS SUPPLY

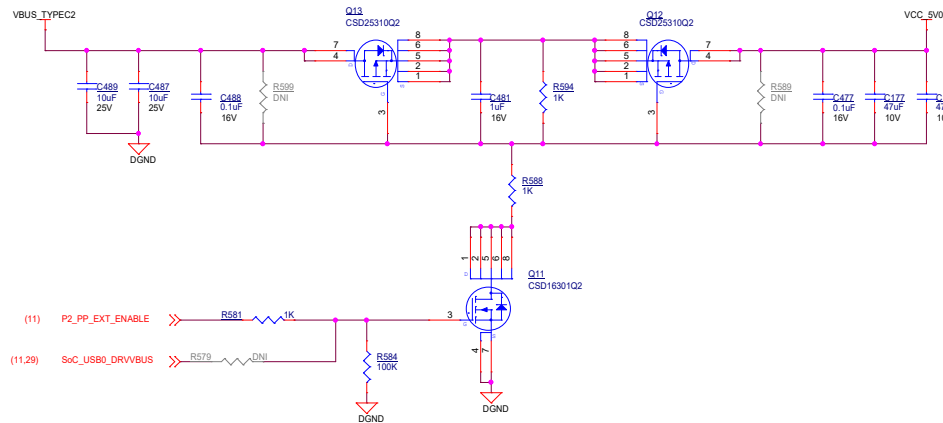


D-Note:-  
Note the assembly related concerns with DQN package.  
Consider using alternate package.

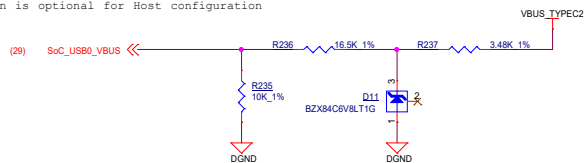
## USB0 TYPE-C DRP



## EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A

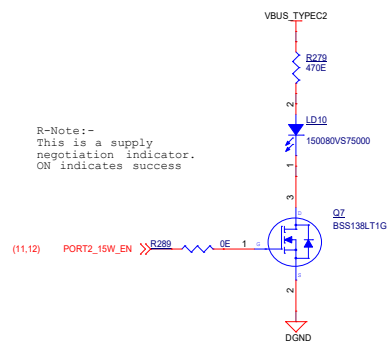


D-Note:-  
VBUS connection is optional for Host configuration



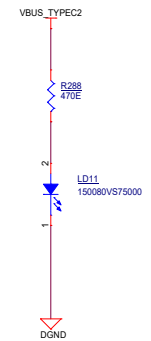
D-Note:-  
Refer USB VBUS Design Guidelines section of SOC data sheet

## PORT2\_15W\_EN STATUS INDICATION LED

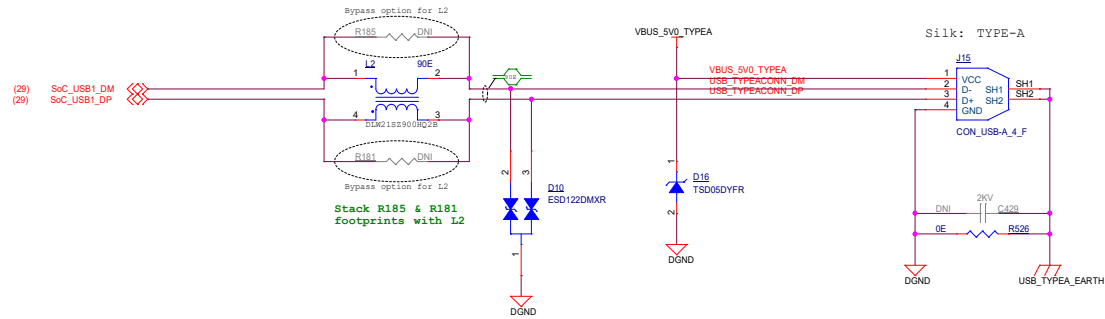
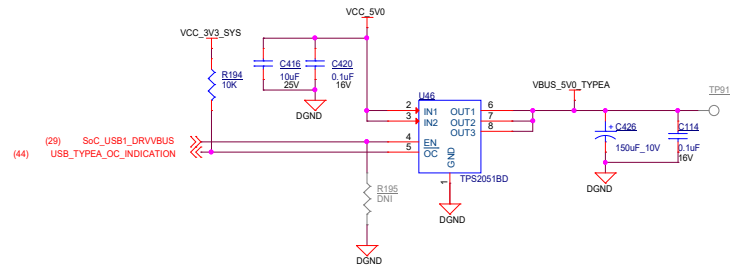


R-Note:-  
This is a supply  
negotiation indicator.  
ON indicates success

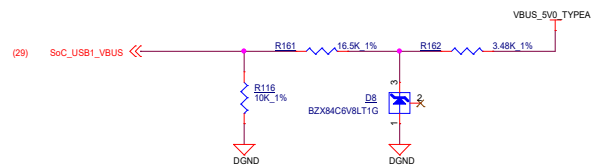
POWER INDICATION LED: VBUS\_TYPEC2



## USB1 TYPE-A

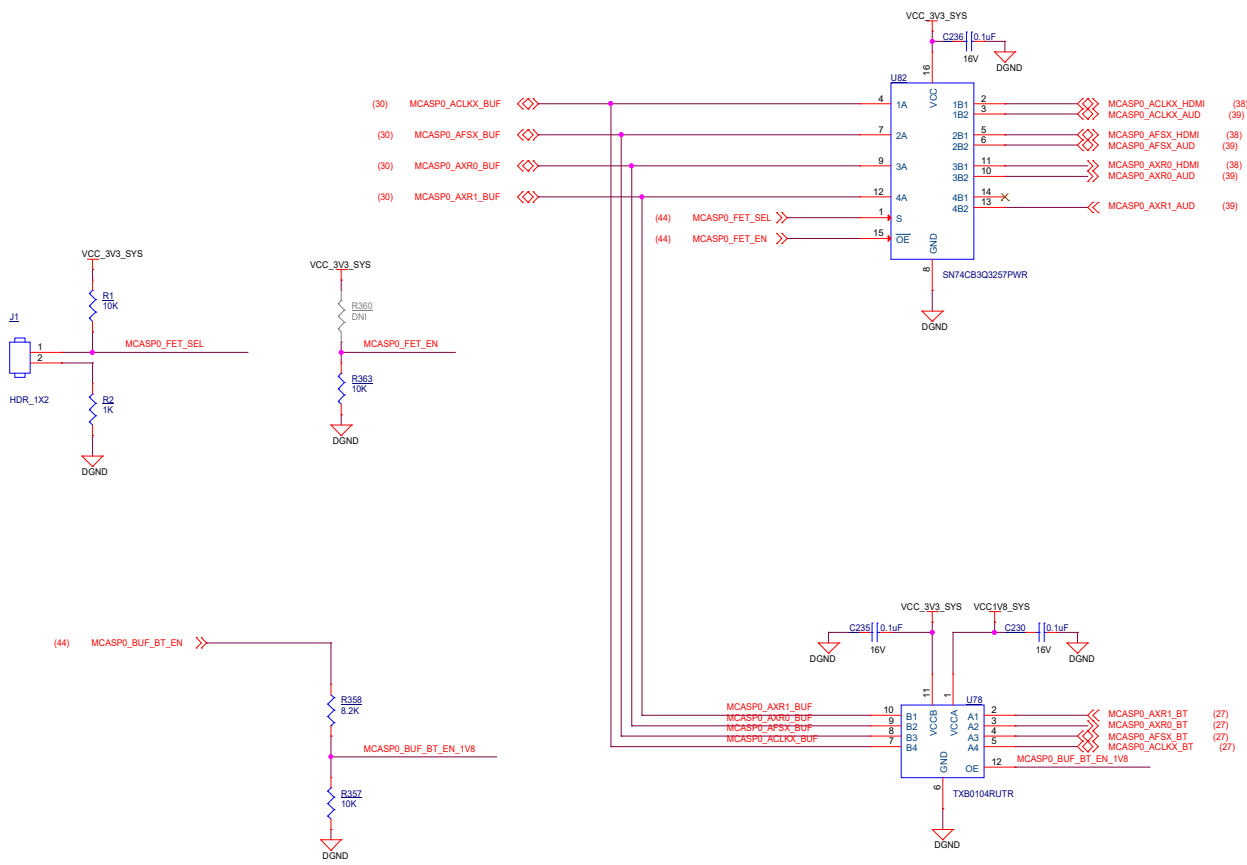


D-Note:-  
VBUS connection is optional for Host configuration

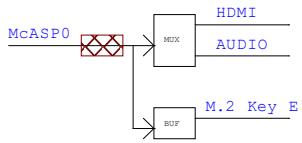


D-Note:-  
Refer USB VBUS Design Guidelines section of SOC data sheet

SOC MAIN McASP0 FET BUS SWITCH & VOLTAGE LEVEL TRANSLATOR



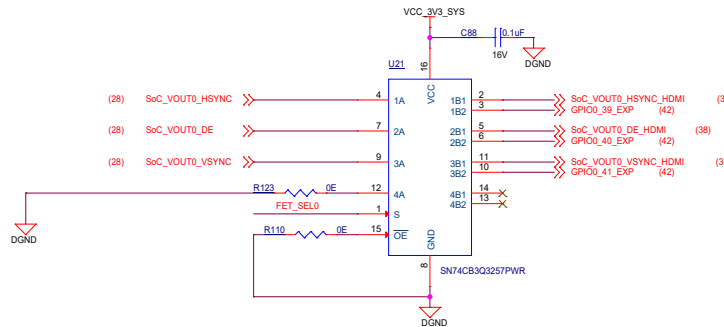
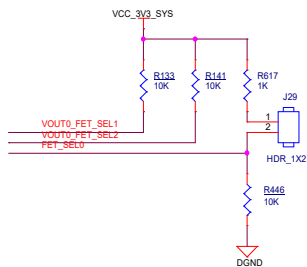
OEn	SEL	INPUT/OUTPUT nA	
L	H (DEFAULT)	nA=nB2	MCASP0 - CODEC
L	L	nA=nB1	MCASP0 - HDMI



# SoC\_VOUT0 FET SWITCHES



S2	S1	S0	INPUT/OUTPUT nA	
H	H	L	nA=nB1	SOC - HDMI (DEFAULT)
H	H	H	nA=nB2	SOC - GPIO EXP CONN



OEn	SEL	INPUT/OUTPUT nA	
L	L	nA=nB1	SOC - HDMI (DEFAULT)
L	H	nA=nB2	SOC - GPIO EXP CONN

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Title SOC VOUT0 FET SWITCHES

Size PROC181E1-1A

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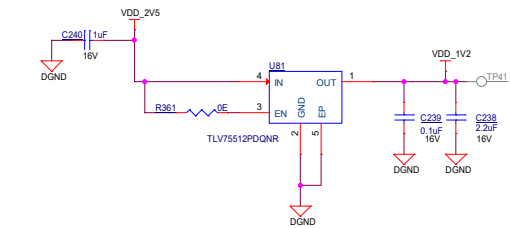
Date: Monday, October 06, 2025

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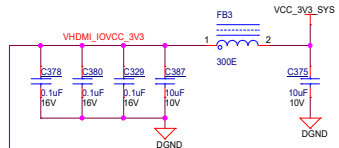
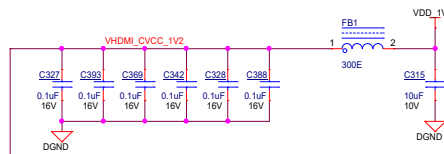
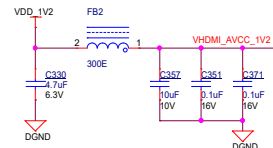
Rev  
E1-1A

# HDMI INTERFACE

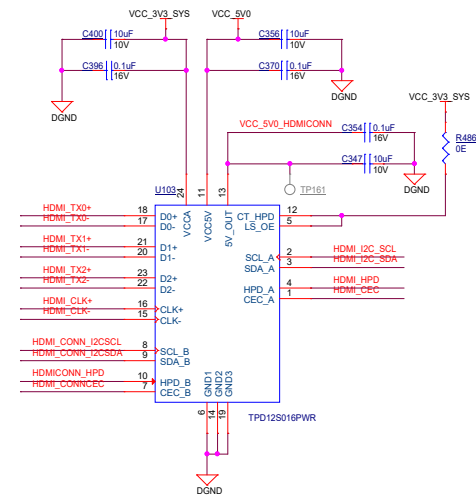
1.2V (HDMI), 0.5AMPS SUPPLY



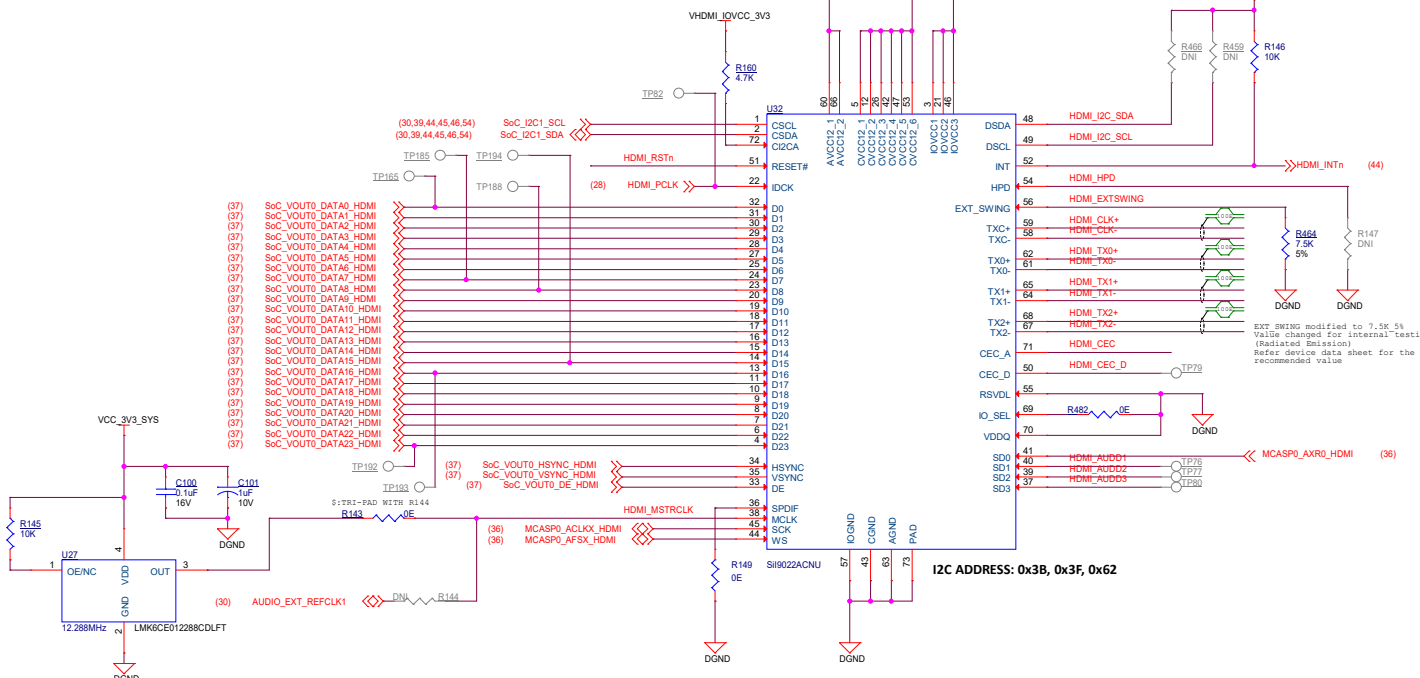
D-Note:-  
Note the assembly related concerns with DQN package.  
Consider using alternate package.



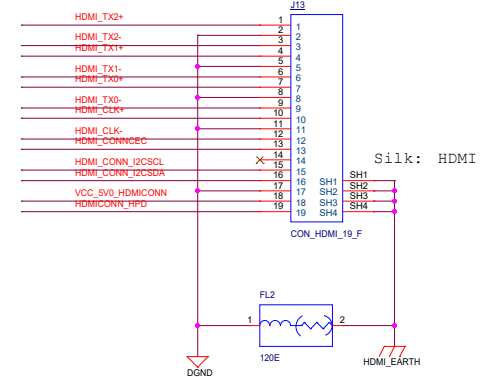
## HDMI ESD DEVICE



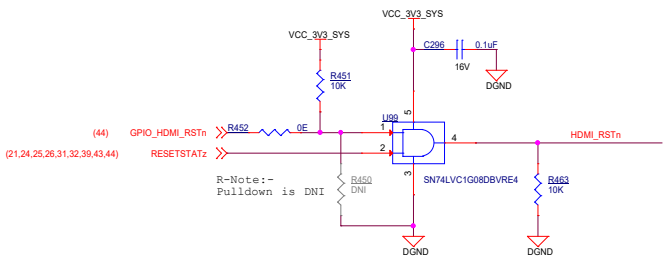
NOTE:  
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.



## HDMI CONNECTOR



## HDMI RESET



(21,24,25,26,31,32,39,43,44)

RESETSTATz

R-Note:- Pulldown is DNI

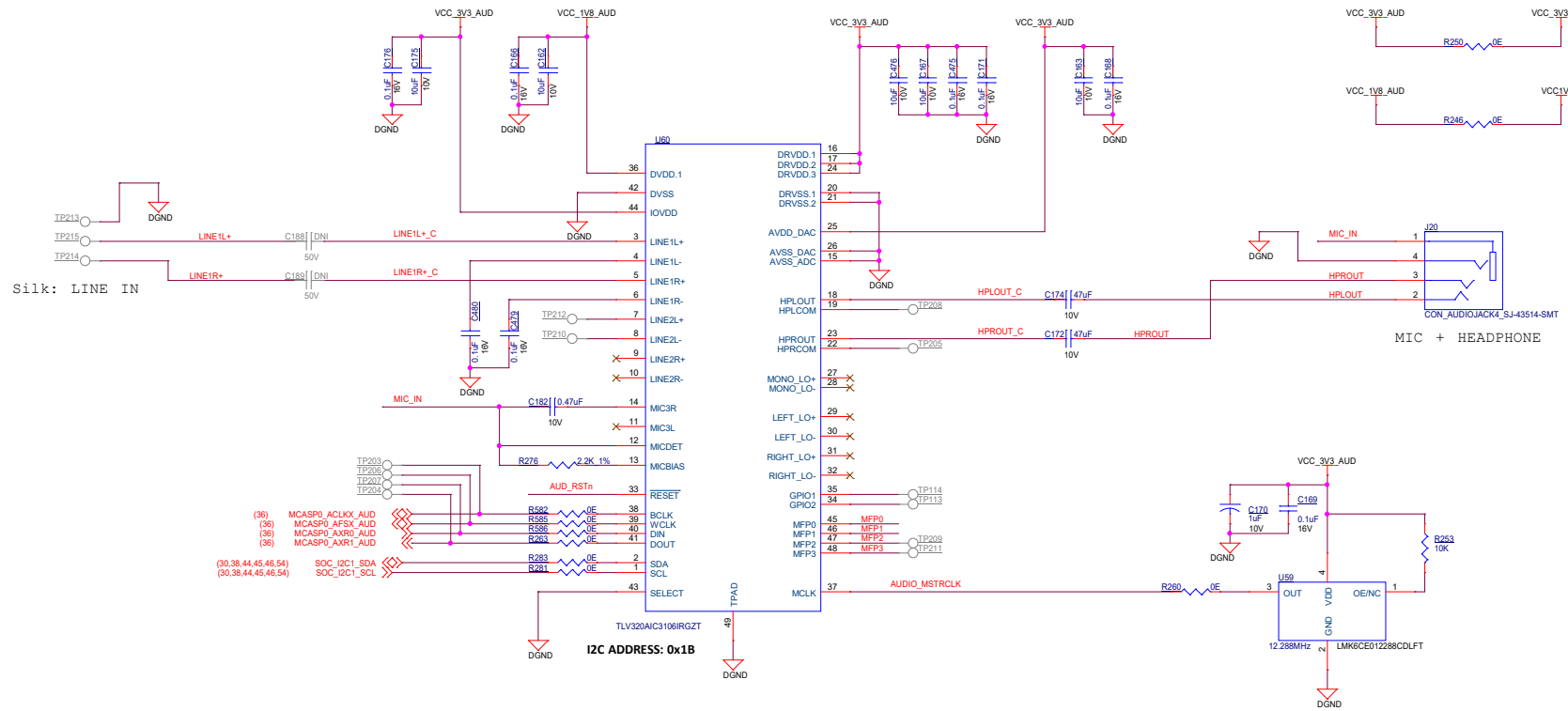
PROC181E1PIA

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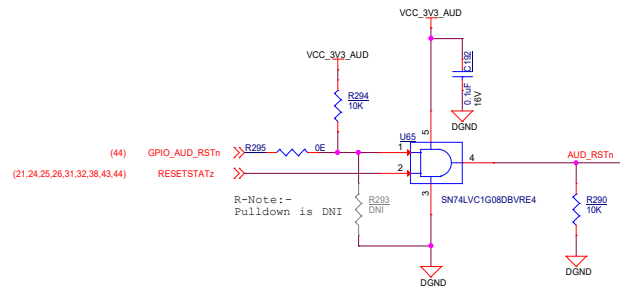


Title			DPI to HDMI TRANSMITTER INTERFACE	
Size	PROC181E1-1A		Rev	
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Date:	Monday, October 06, 2025		Sheet	38 of 56

# AUDIO CODEC

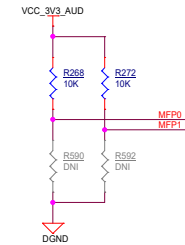


## AUDIO CODEC RESET



## CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



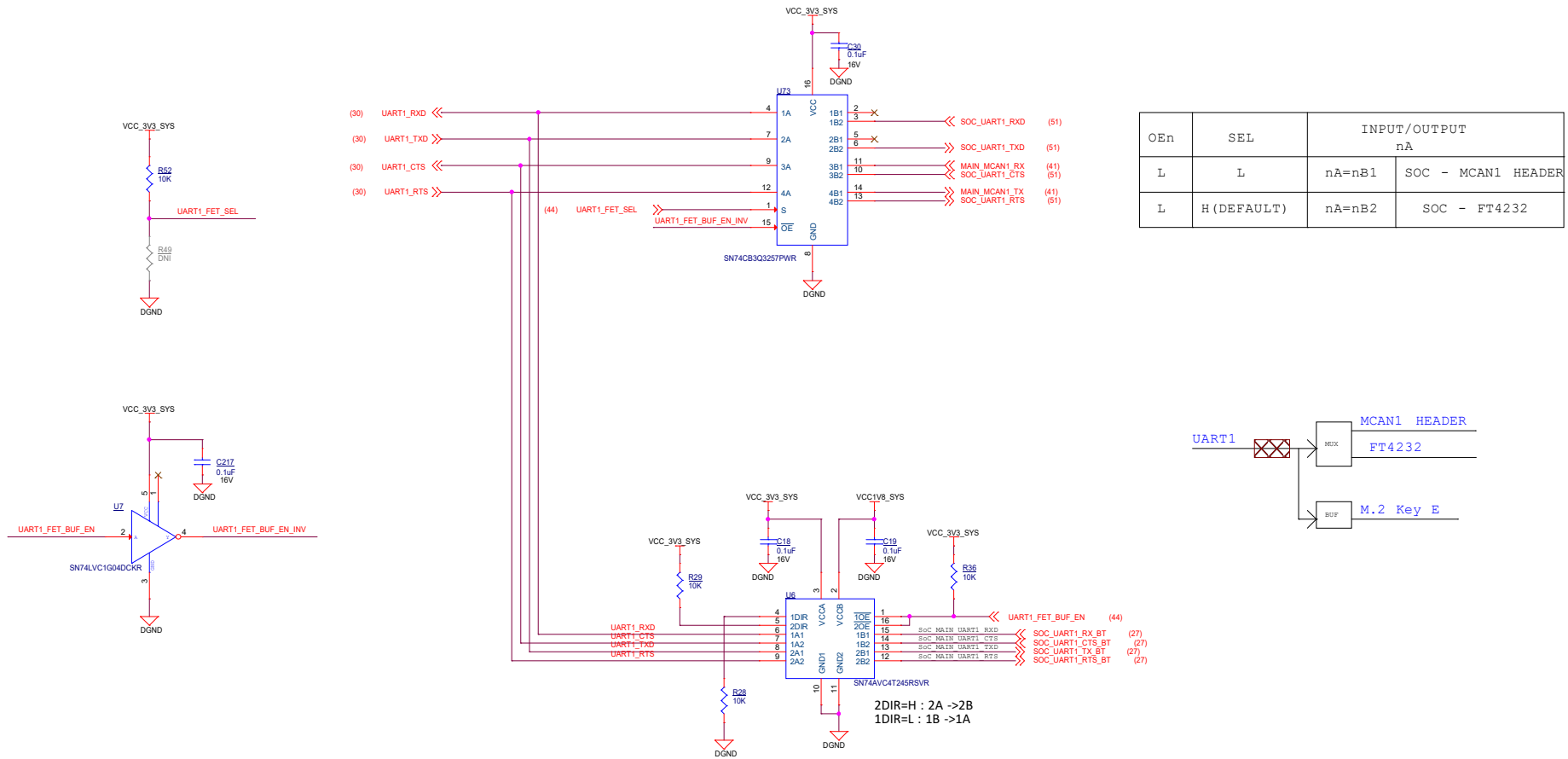
PROC181E1PIA

Designed for TI by Mistral Solutions Pvt Ltd



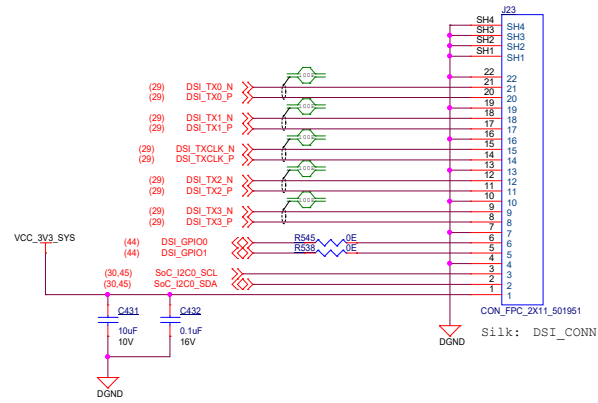
Title		AUDIO CODEC	
Size	PROC181E1-1A	Rev	E1-1A
C			
Date:	Monday, October 06, 2025	Sheet	39 of 56

# SOC MAIN UART1 - FET SWITCH & VOLTAGE LEVEL TRANSLATOR

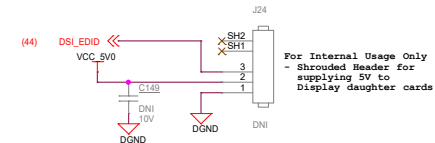




## DSI INTERFACE

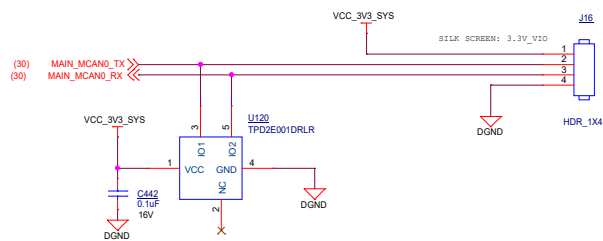


### ADD ON CARD HEADER

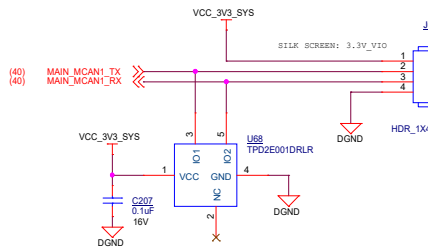


## MCAN INTERFACE

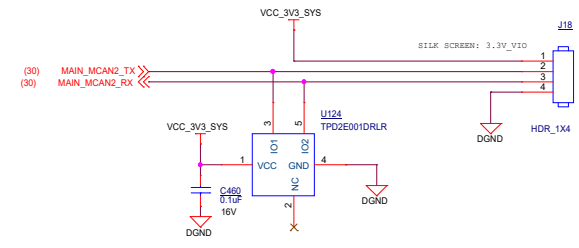
## MCANO HEADER



## MCAN1 HEADER



## MCAN2 HEADER



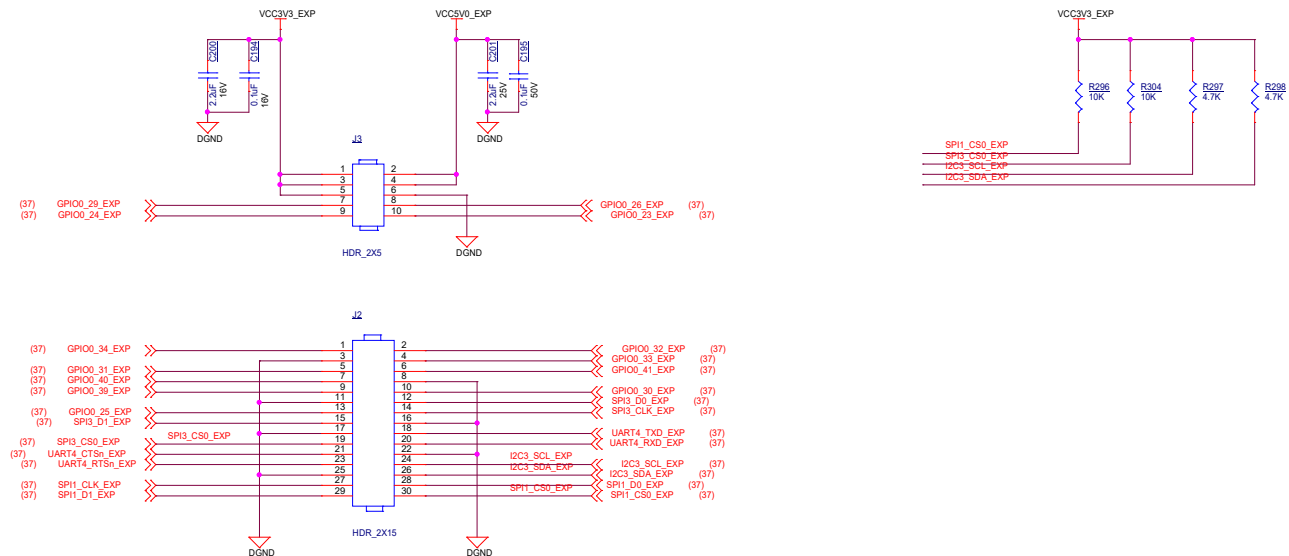
PROC181E1P1A

Designed for TI by Mistral Solutions Pvt Ltd

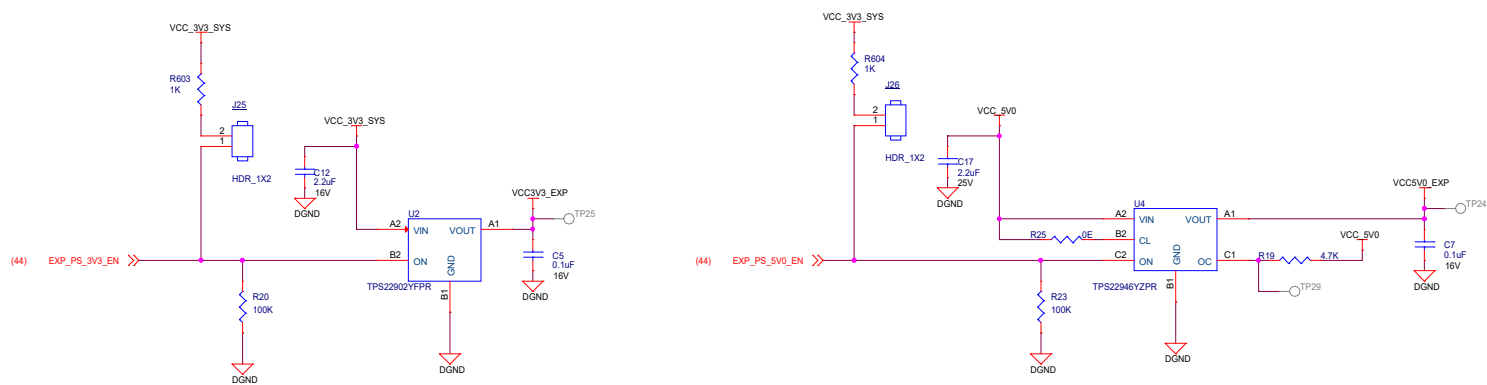


Title				DSI LCD INTERFACE CONNECTOR & EXTERNAL MCAN CONNECTOR			
Size		PROC181E1-1A				Rev	
C						E1-1A	
Date:		Monday, October 06, 2025		Sheet		41 of 56	

# GPIO EXPANSION CONNECTOR



## LOAD SWITCH FOR GPIO EXPANSION CONNECTOR



PROC181E1PIA

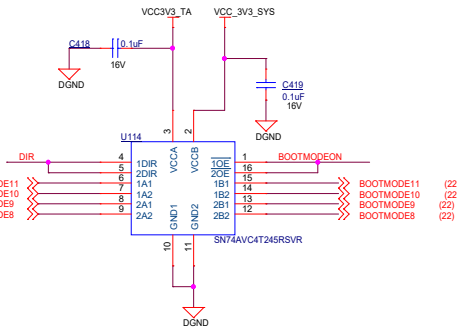
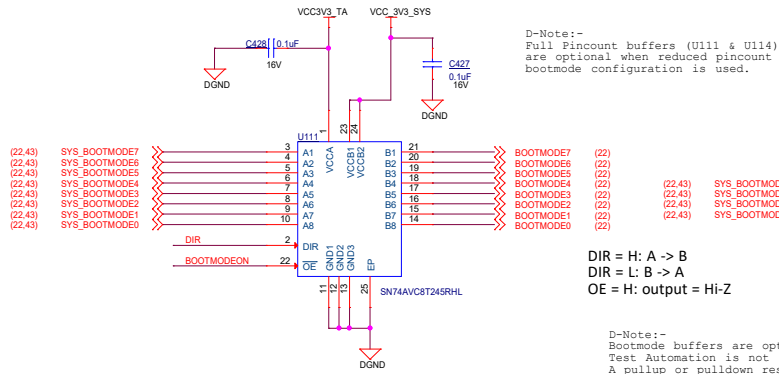
Designed for TI by Mistral Solutions Pvt Ltd



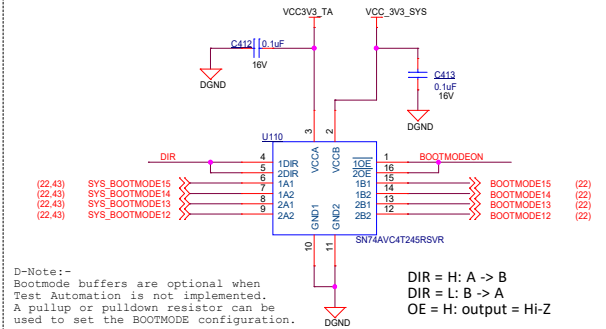
Title		GPIO EXPANSION CONNECTOR	
Size	PROC181E1-1A	Rev	E1-1A
C		Date	Monday, October 06, 2025
Sheet	42	of	56

# BOOTMODE BUFFERS AND IO EXPANDERS

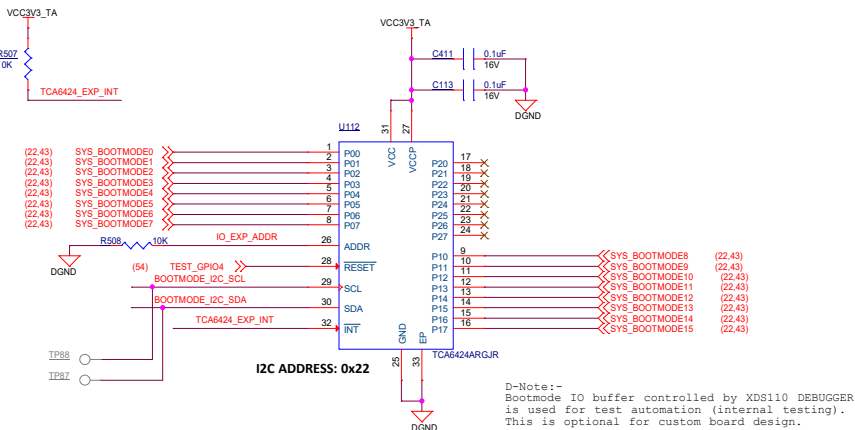
## FULL PINCOUNT BUFFERS



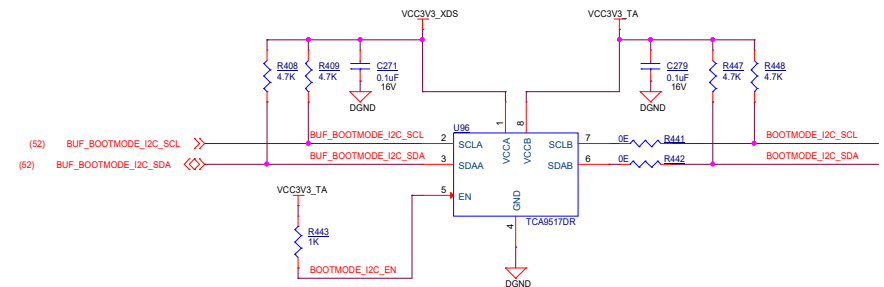
## REDUCED PINCOUNT BUFFER



## BOOTMODE IO EXPANDER



## BOOTMODE I2C BUS BUFFER



PROC181E1PIA

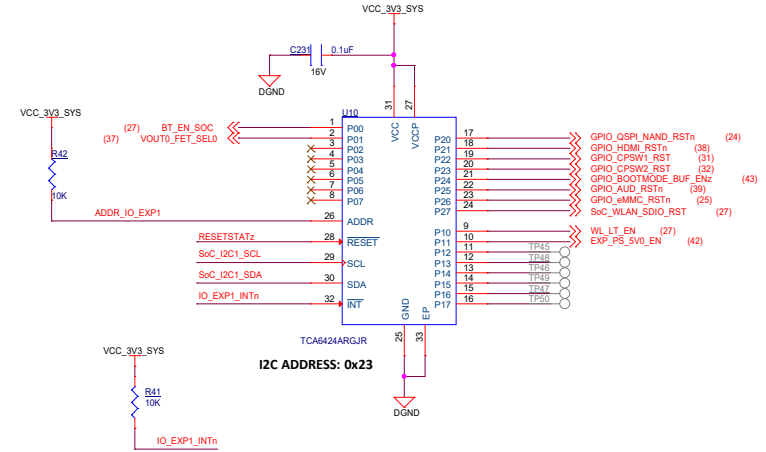
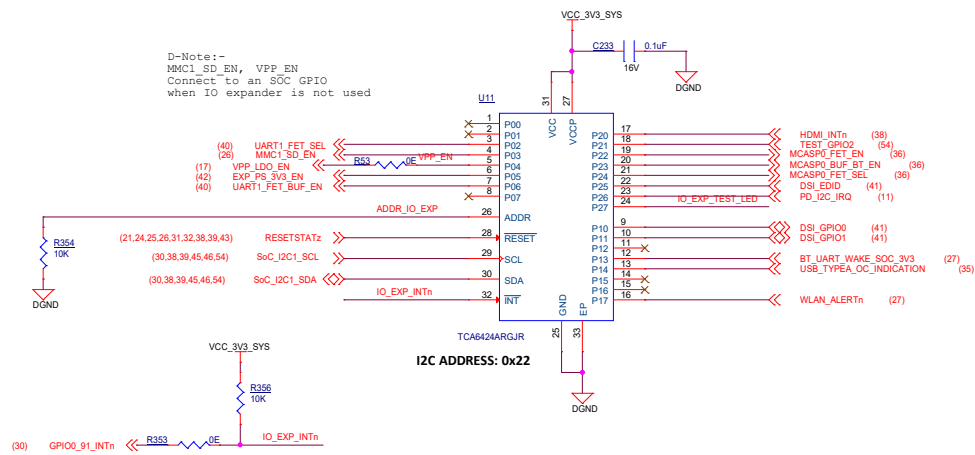
Designed for TI by Mistral Solutions Pvt Ltd



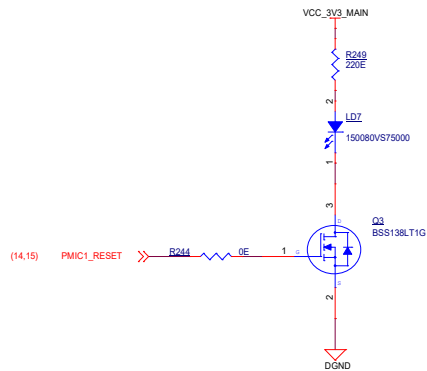
Title BOOTMODE BUFFERS AND IO EXPANDERS

Size	PROC181E1-1A	Rev	E1-1A
C			
Date:	Monday, October 06, 2025	Sheet	43 of 56

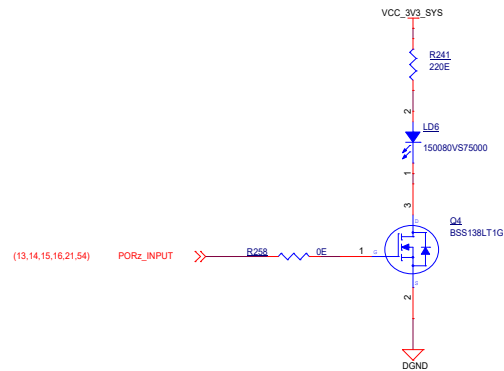
## IO EXPANDERS



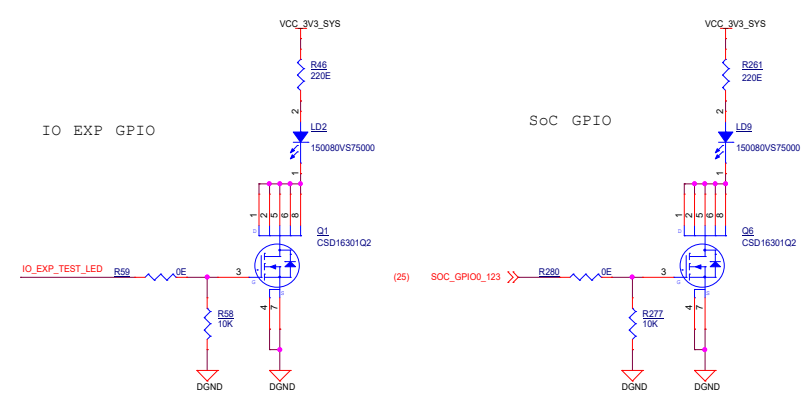
### RTC ONLY MODE INDICATION LED



## POWERGOOD INDICATION LED



## USER TEST LEDS



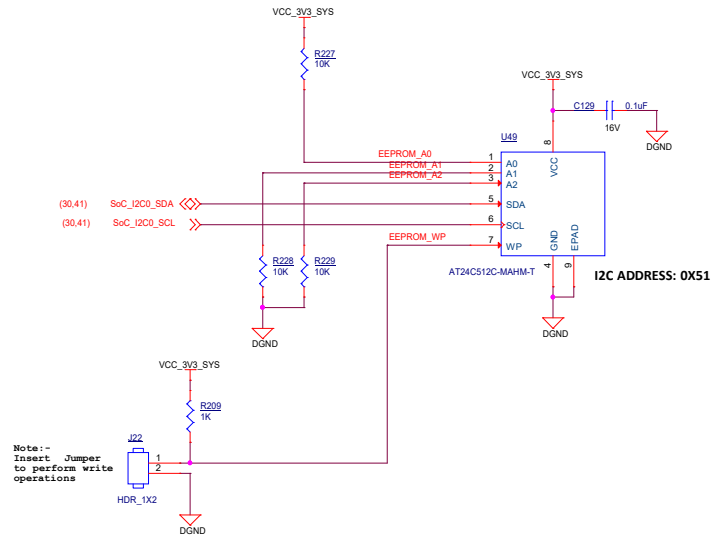
PROC181E1P1A

Designed for TI by Mistral Solutions Pvt Ltd

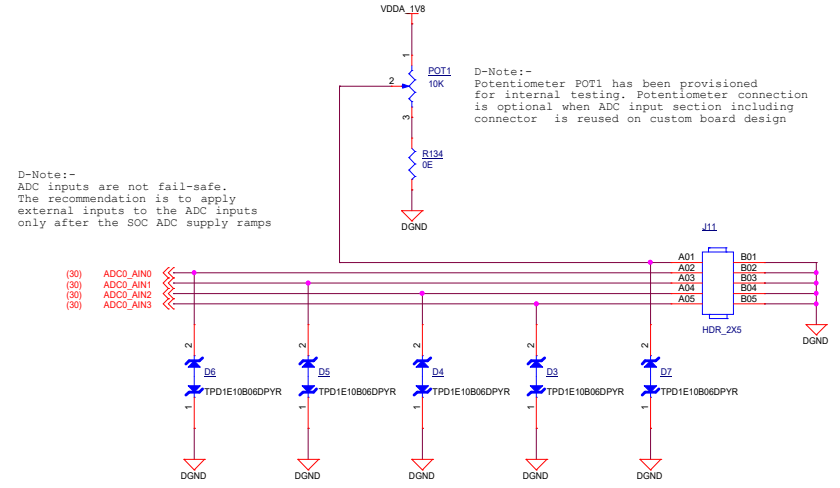


Title				IO EXPANDER & LEDs			
Size		PROC181E1-1A				Rev	
C						E1-1A	
Date:		Monday, October 06, 2025		Sheet		44 of 56	

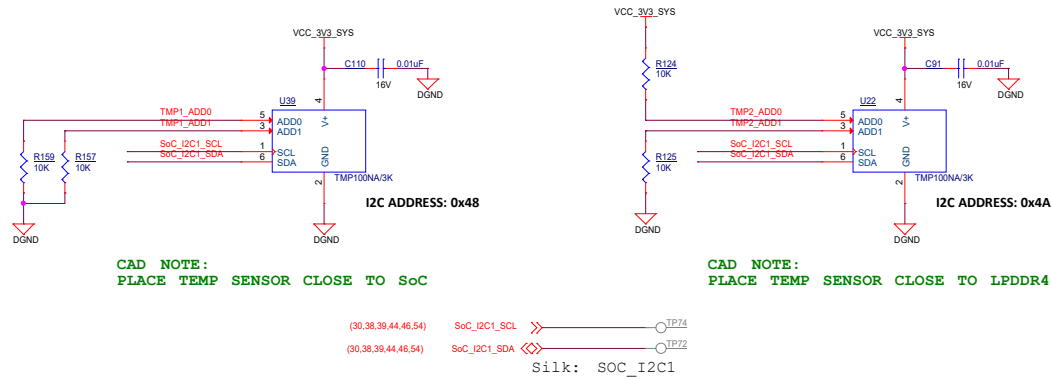
## BOARD ID EEPROM



## ADC INTERFACE



## TEMPERATURE SENSORS



PROC181E1PIA

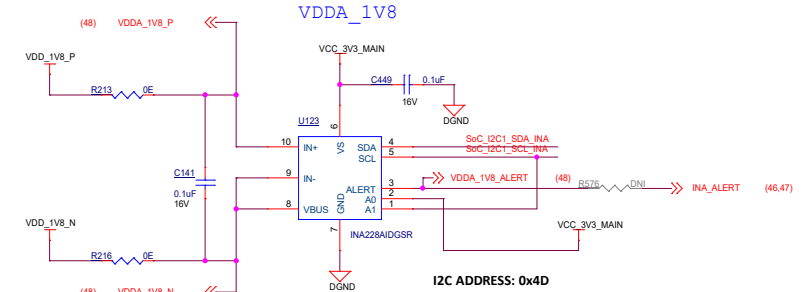
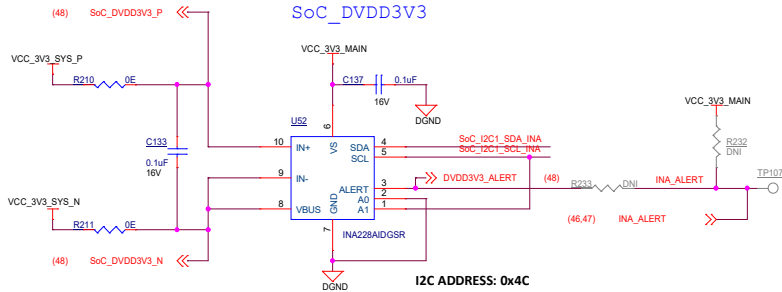
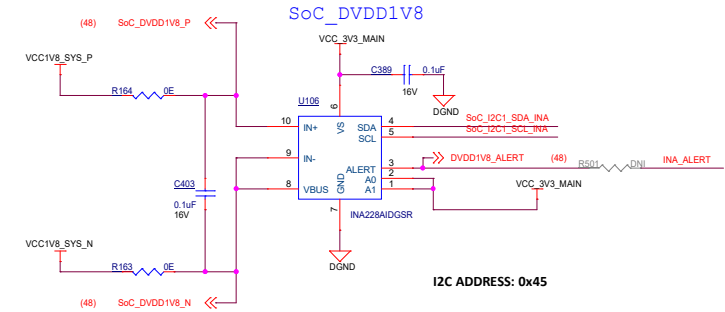
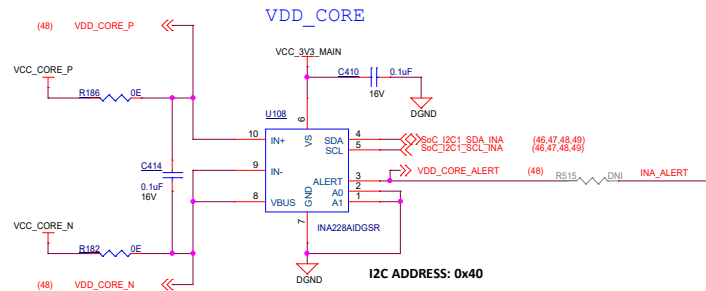
Designed for TI by Mistral Solutions Pvt Ltd



Title			Rev	
BOARD ID EEPROM, ADC INTERFACE & TEMPERATURE SENSORS			E1-1A	
Size	PROC181E1-1A			
C				
Date:	Monday, October 06, 2025	Sheet	45	of 56

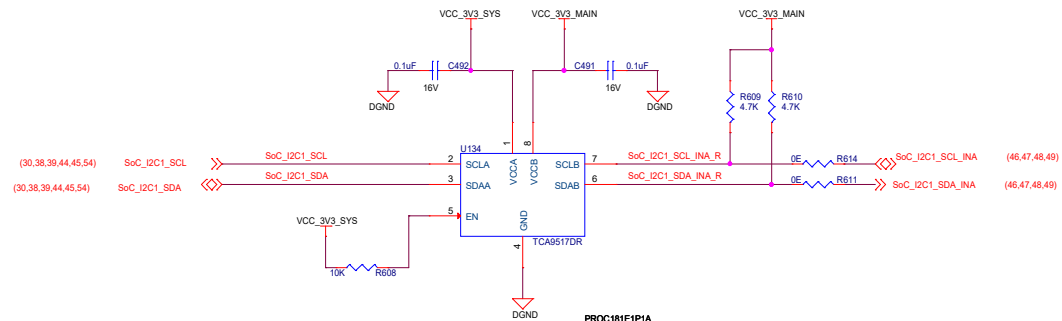
# CURRENT MONITORING DEVICES - 1\_A

CAD Note:  
Follow Kelvin current sense routing while using 2 terminal resistors



**Note:**  
The design supports current/voltage measurements for the on-board supplies using either INA228 or INA231. INA228 will be populated on the EVM (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8_SYS	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1_PMIC1 (From PMIC 1)	VDD_LPDDR4 (From PMIC 1)	47
VCC1V1_PMIC2 (From PMIC 2)	VDD_LPDDR4 (From PMIC 2)	49
SoC_VDD_RTC_HDR	SoC_VDD_RTC	44
SoC_VDDS_RTC_1V8_HDR	SoC_VDDS_RTC_1V8	46



PROC181E1PIA

Designed for TI by Mistral Solutions Pvt Ltd



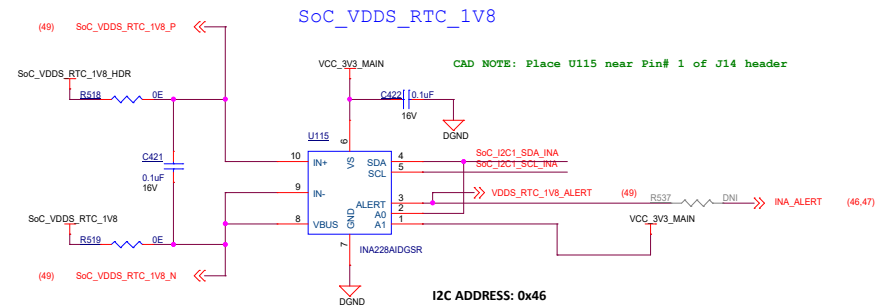
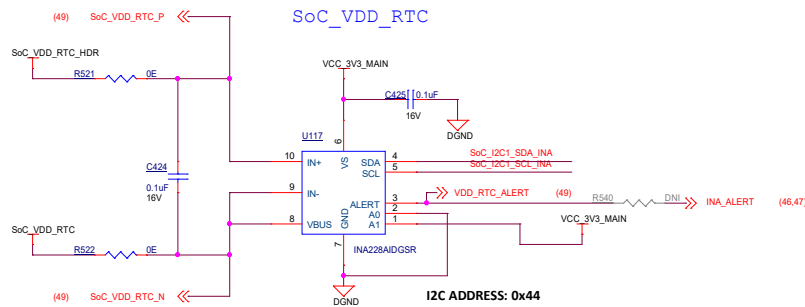
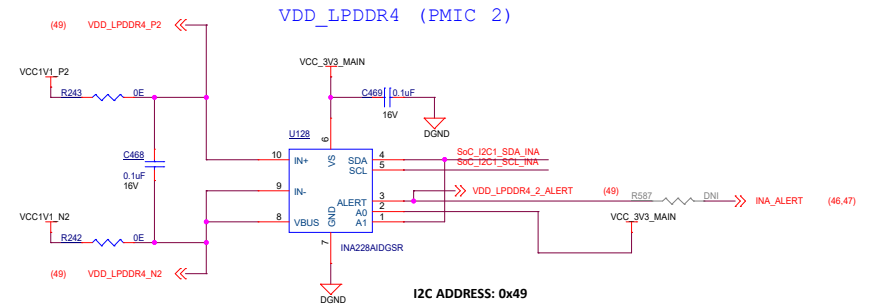
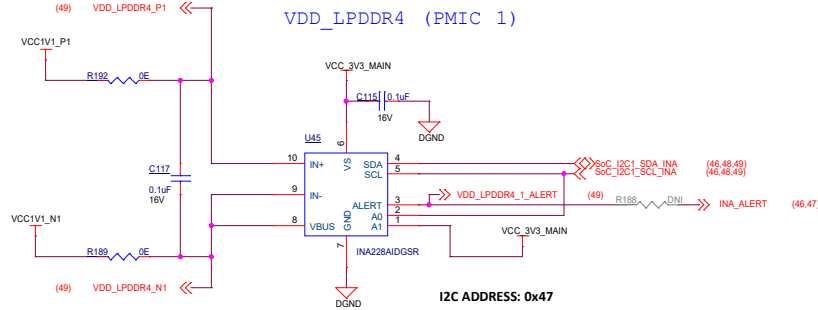
Title CURRENT MONITORING DEVICES - 1\_A

Size	Rev
C	E1-1A
Date:	Monday, October 06, 2025

Sheet 46 of 56

# CURRENT MONITORING DEVICES - 1\_B

CAD Note:  
Follow Kelvin current sense routing while using 2 terminal resistors



Note:  
The design supports current/voltage measurements for the on-board supplies using either INA228 or INA231.  
INA228 will be populated on the EVM (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8_SYS	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1 PMIC1 (from PMIC 1)	VDD_LPDDR4 (from PMIC 1)	47
VCC1V1 PMIC2 (from PMIC 2)	VDD_LPDDR4 (from PMIC 2)	49
SoC_VDD_RTC_HDR	SoC_VDD_RTC	44
SoC_VDDS_RTC_1V8_HDR	SoC_VDDS_RTC_1V8	46

PROC181E1PIA

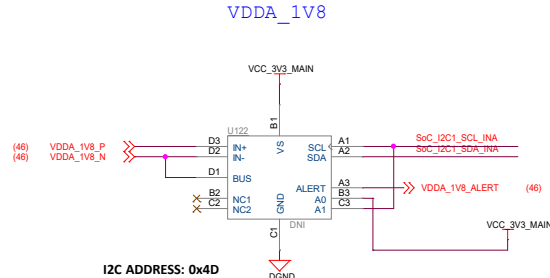
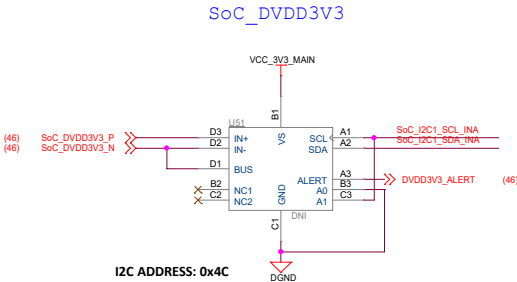
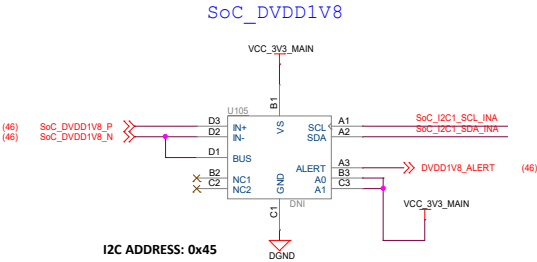
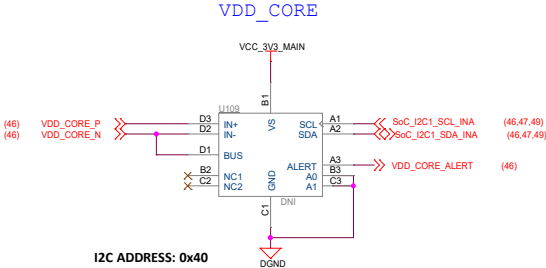
Designed for TI by Mistral Solutions Pvt Ltd



Title CURRENT MONITORING DEVICES - 1\_B

Size	Rev
C	PROC181E1-1A
Date:	Monday, October 06, 2025
Sheet	47 of 56

CURRENT MONITORING DEVICES - 2\_A

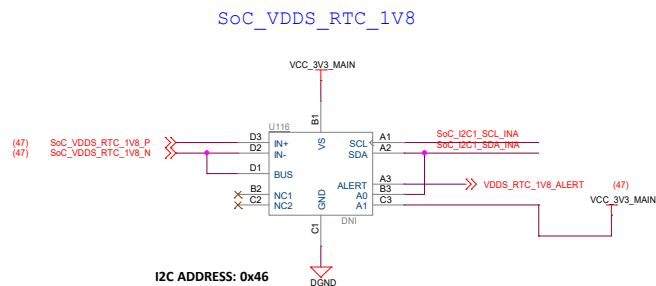
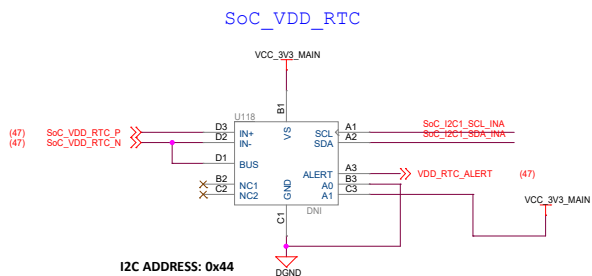
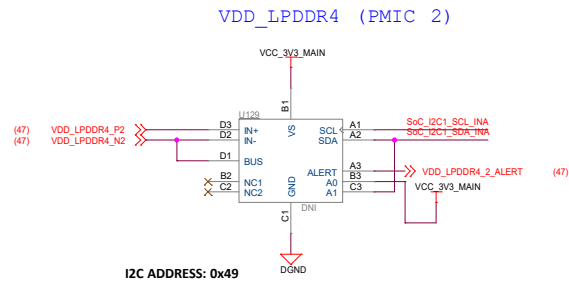
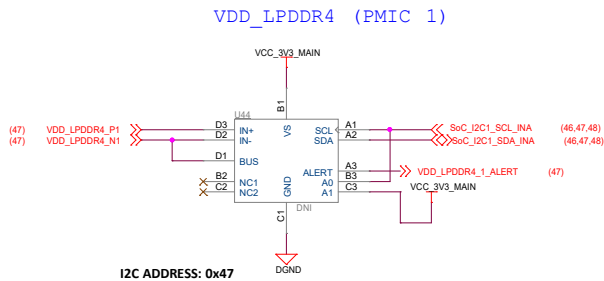


**Note:**  
The design supports current/voltage measurements for the on-board supplies using either INA228 or INA231. INA228 will be populated on the EVM (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8_SYS	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1_PMIC1 (from PMIC 1)	VDD_LPDDR4 (from PMIC 1)	47
VCC1V1_PMIC2 (from PMIC 2)	VDD_LPDDR4 (from PMIC 2)	49
SoC_VDD_RTC_HDR	SoC_VDD_RTC	44
SoC_VDDS_RTC_1V8_HDR	SoC_VDDS_RTC_1V8	46



# CURRENT MONITORING DEVICES - 2\_B



**Note:**  
The design supports current/voltage measurements for the on-board supplies using either INA228 or INA231. INA228 will be populated on the EVM (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8_SYS	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1_PMIC1 (From PMIC 1)	VDD_LPDDR4 (From PMIC 1)	47
VCC1V1_PMIC2 (From PMIC 2)	VDD_LPDDR4 (From PMIC 2)	49
SoC_VDD_RTC_HDR	SoC_VDD_RTC	44
SoC_VDDS_RTC_1V8_HDR	SoC_VDDS_RTC_1V8	46

PROC181E1PIA

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Title CURRENT MONITORING DEVICES - 2\_B (ALTERNATIVE)

Size PROC181E1-1A

C

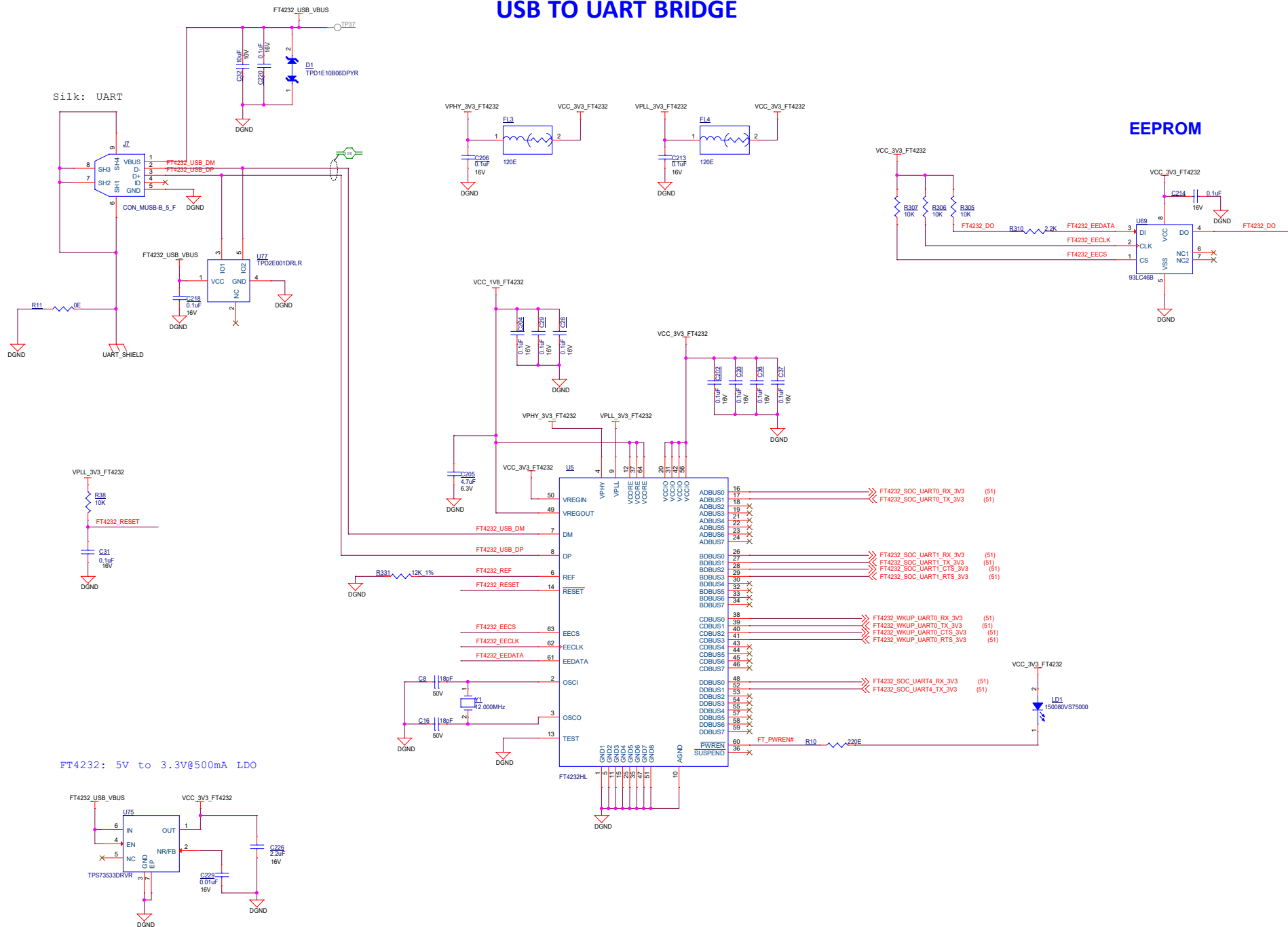
Date: Monday, October 06, 2025

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Rev

E1-1A

## USB TO UART BRIDGE



PROC181E1P1A

Designed for TI by Mistral Solutions Pvt Ltd



Title	USB TO FT4232 UART BRIDGE
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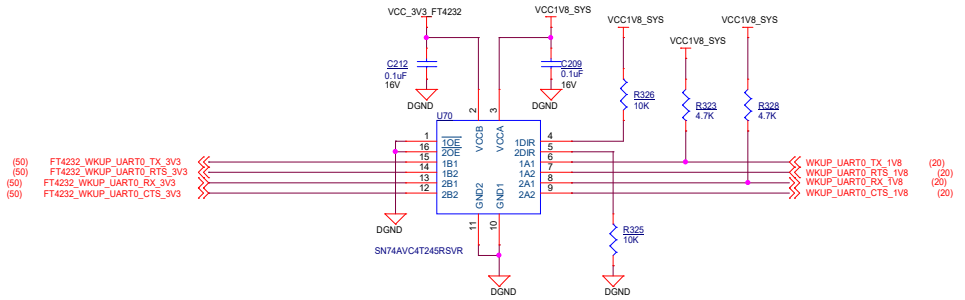
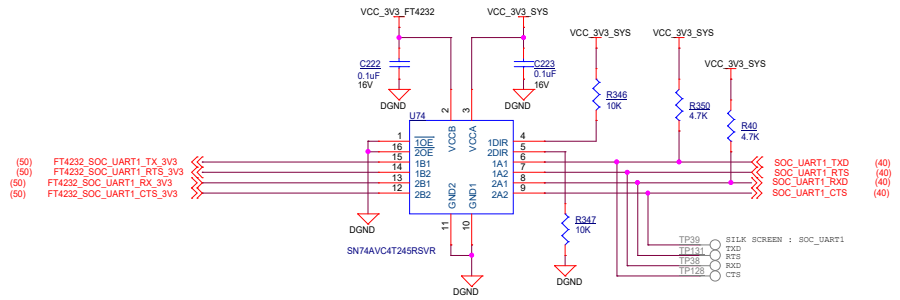
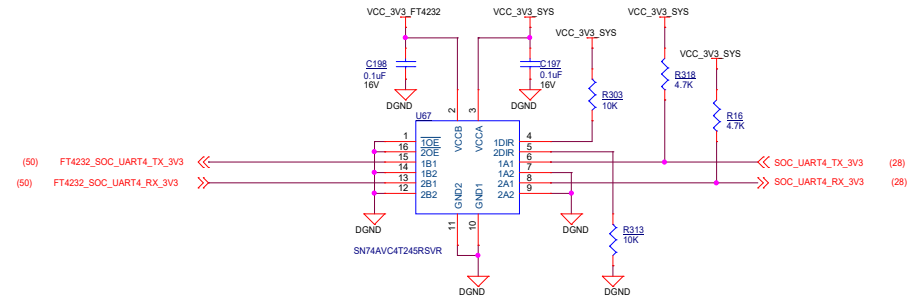
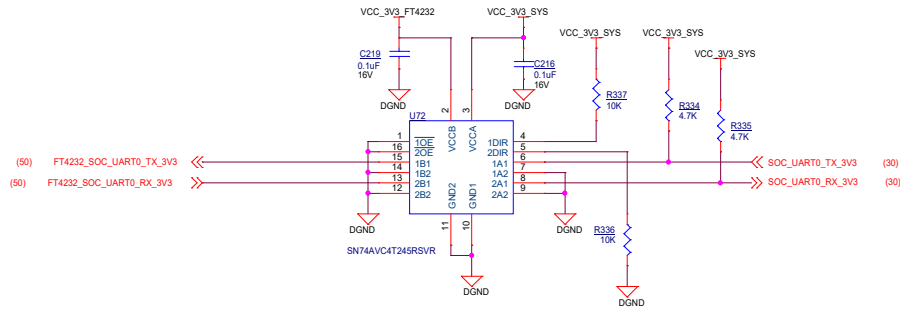
Size	PROC181E1-1A
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Date: Monday, October 06, 2025

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# FT4232 UART BUFFERS



PROC181E1PIA

Designed for TI by Mistral Solutions Pvt Ltd



Title FT4232 UART BUFFERS

Size PROC181E1-1A

C

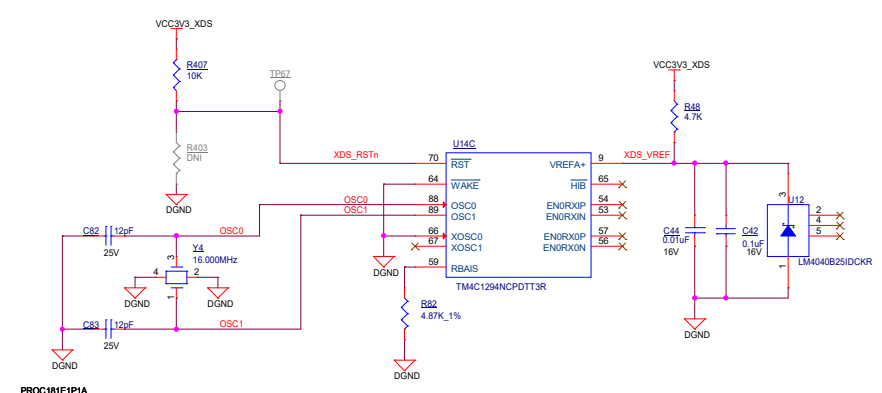
Date: Monday, October 06, 2025

Sheet 51 of 56

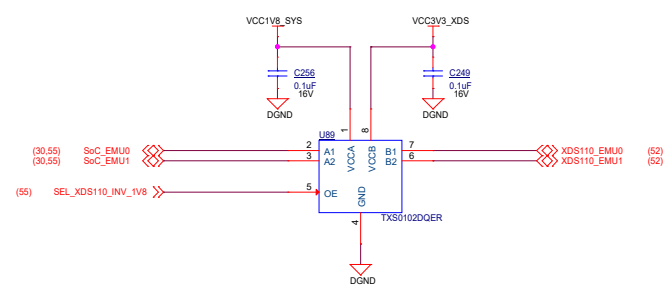
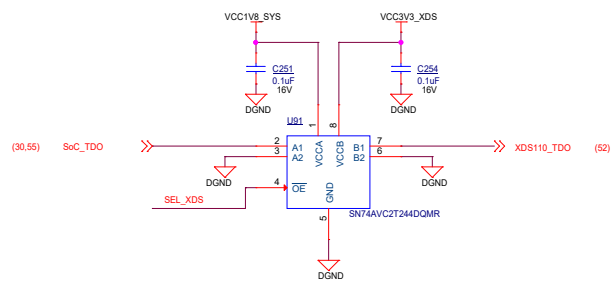
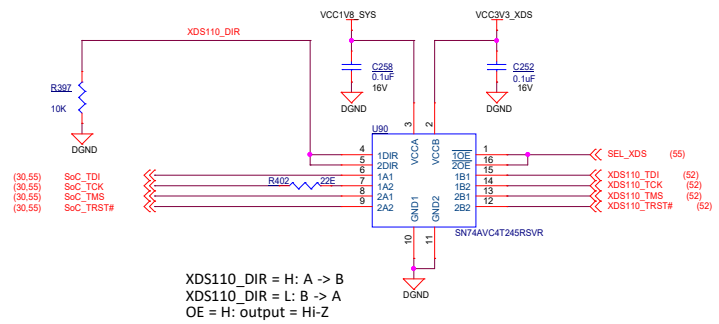
Rev E1-1A

# TEST AUTOMATION GPIO MAPPING

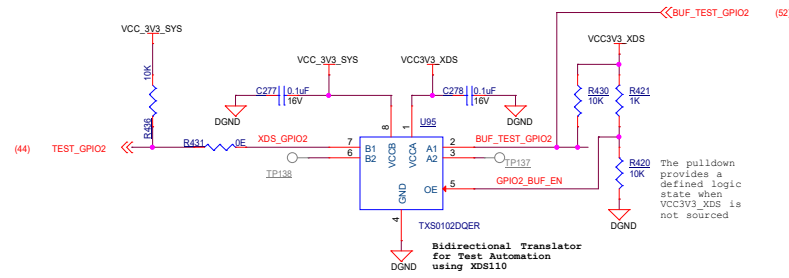
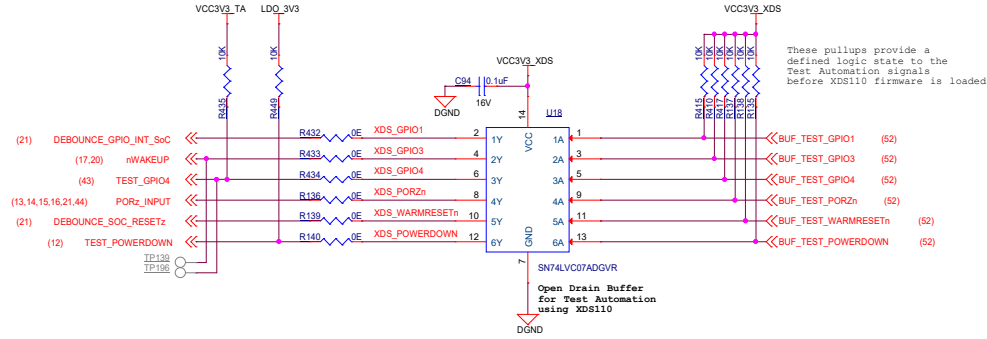
SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETh	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_90 Pin of SoC	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used as nWAKEUP signal of SoC	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup



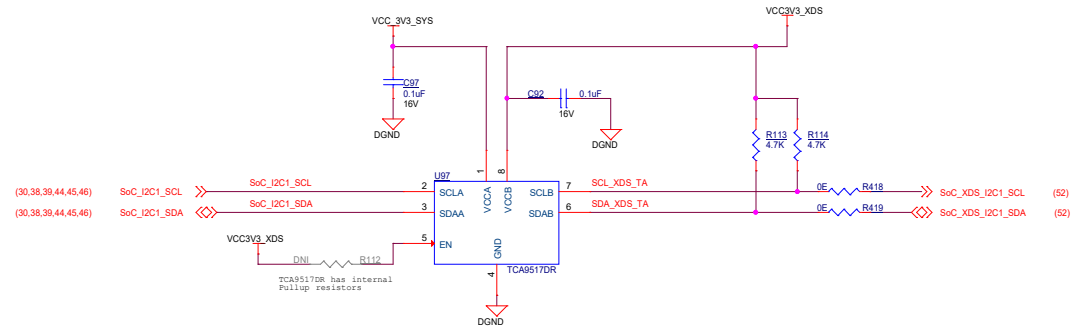
XDS110 JTAG BUFFER



# XDS110 TEST AUTOMATION BUFFERS



## SOC I2C BUS BUFFER



PROC181E1PIA

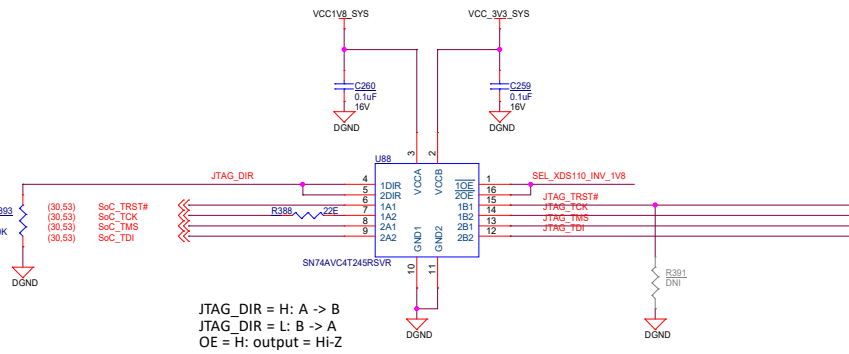
Designed for TI by Mistral Solutions Pvt Ltd



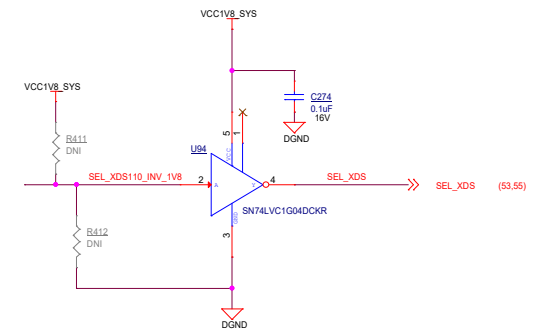
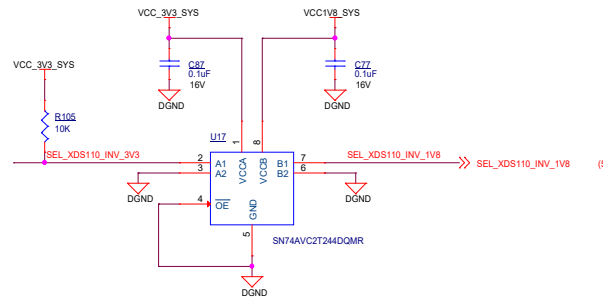
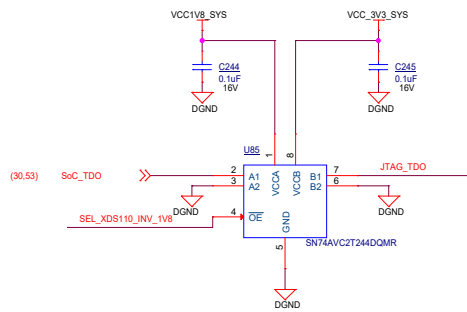
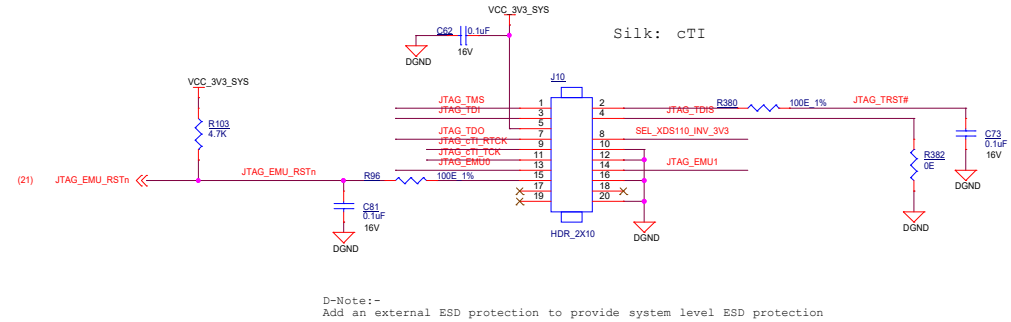
Title XDS110 TEST AUTOMATION BUFFERS

Size	PROC181E1-1A	Rev
C		E1-1A
Date:	Monday, October 06, 2025	Sheet 54 of 56

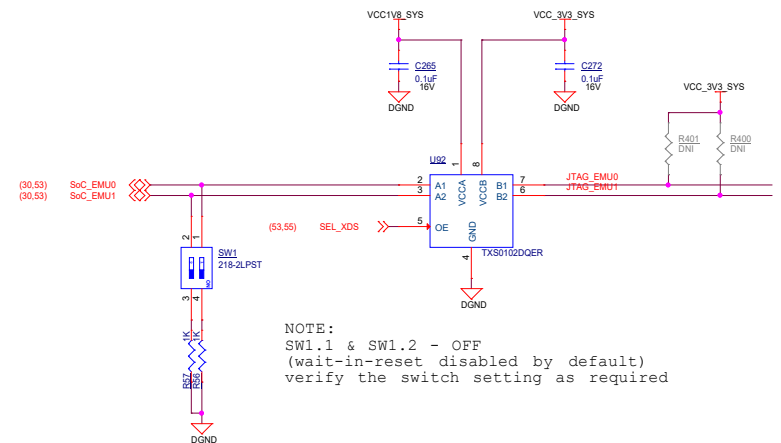
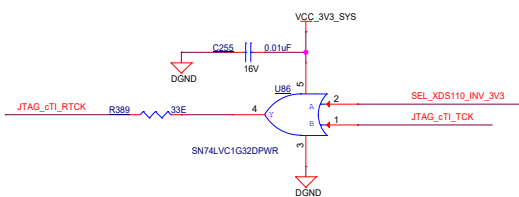
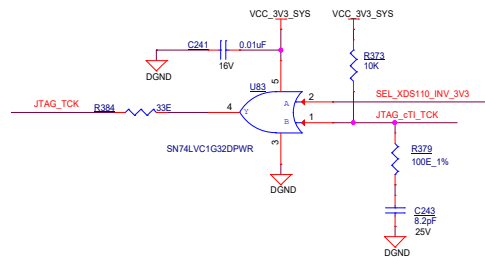
## JTAG2 BUFFERS



## cTI20 JTAG CONNECTOR



## JTAG2 CLOCK BUFFER



PROC181E1PIA

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Title JTAG 20 PIN cTI CONNECTOR

Size PROC181E1-1A

C E1-1A

Date: Monday, October 06, 2025

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Rev

MOUNTING HARDWARE

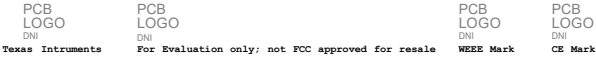
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB



LOGOs



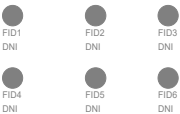
AM62L SOCKET



JUMPERS



FIDUCIALS



LABELS



SCREW & WASHER FOR PCIe M.2



HOUSING & CRIMP FOR DSI HEADER

